CIRCUIT DESCRIPTIONS
Although the RSD-10 has both sampler and delay capabilities, the following description mainly concentrates on sampler feature, assuming that most of readers are familiar with the basic of digital delay circuit which is well explained on the service notes of Roland SDE-1000/3000, Boss DE-2, etc.

SAMPLER RECORDING MODE Fig. 1
The input audio signal coming into S/H (IC1 pins 1 and 3 of Sub board) is passed onto the next stage on a TRIGGER pulse (RECORDING START, causing COST) which enables the Main Controller IC9 to start timing the recording circuits. The trigger pulse is derived from:
- Input audio signal proper--in MODE A (Auto Recording mode)
- External control signal (keyboard, pad or pedal)--in MODE B (Manual Recording mode)

Upon receiving a RECORDING START (COST) signal through Counter Start/Stop Controller (detailed in COUNTER START/STOP section), the Main Controller IC9 coordinates the following processes on the audio input signal. The processing timing being based on the master clock, which in turn is controlled from Keyboard Interface. See these sections for detail.

Sample and Hold circuit for extracting an instantaneous amplitude of the audio signal
Analog-to-Digital Converter (ADC) for obtaining the numerical data to the audio amplitude in PCM form.
Storing of the PCM data into the RAMs IC11 - IC16 for later retrieval.

サンプラー録音時の動作 Fig. 1
INPUT ジャックから入力された信号は常にA/D/A回路 S/H に加えられているが、トリガ信号（録音スタート信号）が加えられなければ、それ時点の入力信号は動作しません。
トリガ信号（録音スタート信号）は、
○モードA（自動録音）の場合\neys録音入力信号から作られる。
○モードB（手動録音）の場合\neys録音入力信号から作られる。
トリガ信号が入ると入力信号は、
- S/H で時定数に基づく。
- A/Dコンバータで2次のデルタに変換される（PCM）。
- RAM（IC11 - IC16）に書き込まれる。
これによりメモリストアに記録され、その後の
タイミングはキーボードインターフェース回路からのビッチコントロール信号によって決まる。

SAMPLER PLAYBACK MODE Fig. 2
There are combinations in sampler playback mode:
- MODE A
- MODE B
- MODE C

MODE A with a Dynamics keyboard control
- MODE D with a Pad or Pedal control

サンプラー再生時の動作 Fig. 2
再生モードにはトリガ再生モード（TRIG）やゲート再生モード（GATE）があります。
トリガ再生モード（TRIG）では
- ダイナミクスによる再生（モードAの場合）
- プロックによる再生（モードBの場合）

トリガ再生モードのヒットコントロールによる再生（MODE D）
- キーボードからのオーウォータ信号は、キーボードインターフェースで3種類の信号に変換されます。
- ボリュームコントロール信号 - IC3（ダイナミックセッサ）を制御する関係によりサンプリング
音の音量を制御する。
- ビッチコントロール信号 - メモリに記録されている
サンプリング音データの読み出し速度を制御する。つまり、サンプリング音の音
を制御する。
この図はキーボード入力を音量コントロール信号へ変換するのに用いる。PLL回路部分を除外した図に、PLL内でのVCOの時定数を考慮して設計する。従来のVCOの設計では、高音域での応答性を高くするため、VCOの時定数を小さく設定していた。しかし、低音域での応答性を向上させるため、VCOの時定数を大きく設定することが必要である。この図はVCOの時定数を大きく設定することで、低音域での応答性を向上させた設計を示している。
PLAYBACK TRIM Fig. 5

This circuit determines the reproduction period of sampled sound. At the same time the sampler playback starts, the 15-bit binary counter (IC10 and IC12) is reset on a COUNTER RESET signal and starts counting the PITCH CONTROL (sampling clocks). The 8-bit counts from the counter causes the DAC (RA1) output voltage to ramp from 2V toward 7V. Since the intervals of the sampling clocks and the memory address steps are the same, the DAC output ramp time can be correlated with the RAM memory length; 7V being the end of memory address. The comparator IC13A turns Q22 off when the DAC output voltage exceeds the voltage set by PLAYBACK TRIM, shutting in the sampled sound.

DYNAMICS SENSOR Fig. 6

This circuit controls the volume of sampled sound, with the control voltage derived from a keyboard audio signal or a pad. Exampled in Fig. 6 is the flow of control signals when in mode (GATE PLAY) with the volume of a sampled sound being controlled from a dynamics keyboard. The VOLUME CONTROL signal from the Keyboard Interface is rectified and applied to the variable gain cell (VCA). The VOLUME CONTROL signal is replaced by the voltage from Q9 of Pad Interface when pad output is fed to PAD IN jack in sampler A, B, or C modes. If the PAD IN jack is not engaged in either of these modes or delay mode, IC3 is kept at the fixed gain determined by the BIAS VOLTAGE on pin 1.

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**MASTER CLOCK GENERATOR**

Master Clock Generator IC10a, b starts oscillation on the positive going edge of PITCH CONTROL signal from the Keyboard Interface, output frequency being approximately 5MHz.

The Main Controller I9, when being fed with the MASTER CLOCKS, completes a cycle of writing or reading of the RAM memory by the 64th clock and swings SAH to high. The SAH resets the Master Generator and keeps it at rest till another low to high transition of PITCH CONTROL occurs. In this way, although the frequency of the MASTER CLOCKS remains constant the frequency of clocks of the timing generator inside the Main Controller varies in proportion to the change of PITCH CONTROL frequency. The clock rate of the timing generator determines the timing of ADC, DAC, S/H and RAM access. Therefore, when the PITCH CONTROL lowers in frequency, the clock rate of the timing generator lowers and consequently the pitch of sampled sound also lowers.

**COUNTER START/STOP**

This circuit handles the start/stop of the memory address counter in the main controller I9. Whenever a TRIGGER pulse is applied to the base of Q4, it causes IC7a and b to have pulses of opposite polarity. The COUNTER START signal on pin 5 of IC7a and d enables them to generate pulses of Q (L to H) and Q (H to L). Q removes COUNTER STOP (COST), allowing IC9 to access to the beginning of memory address (RAMs IC11 - IC16). At the end of memory address, IC9 pulls TEMP low, signaling the IC7a, d to generate a COUNTER STOP signal (Q = L to H). This memory access cycle of one trigger/pulse cycle can be interrupted by a new TRIGGER pulse input during memory access: In this case only COUNTER RESET from pin 3 of IC7a to DATA of IC9 is active; IC9 skips the remaining addresses and jumps to the beginning of the address. In the DELAY mode COST of IC9 is permanently pulled up, deactivating COUNTER STOP, even if developed.

**A/D MODE**

Placing MODE at A keeps the two FFs of IC8 in the reset status. Upon receiving a sufficient level audio signal, Audio DEC IC6 and Q2 applies a low to S of IC8a and b which generates AUTO START trigger pulse. The Q4 and IC7a, d response to this trigger pulse as mentioned previously: removal of COST (H to L). The main controller IC9 starts storing data to RAMs, and when completes accessing to all memory cells develops TEMP: IC7a, d pulls its Q low (COST STOP): IC8c, d swings its Q output high (HOLD). IC9 transfers this hold HIGH to its WRITE pin, protecting RAMs from being rewritten over the existing data.

To release write protection, MODE switch must be set temporarily to B, then again to A.

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**INFORMATION**

모드스위치는[그림]에나 정해져 있는 것과 IC8 내의 2개의 FF는 리셋 상태인 것이다. 입력 신호가 높으면, 오토스트레트 스타트 신호가 IC8a, b의 S에 들어가, 오토스트레트 트리거가 발생할 것이다. 이로 인해 IC7a, d의 Q 출력이 높아지지 않게, COST가 해제된다. MODE 인터페이스의 FF는 잠재적으로 IC9에서 발생하는 TEMP의 효과로 IC7a, d가 캐운타사트 스타트 신호를 IC8c, d에 전달한다. IC8c, d의 Q 출력은 F로 되고, 다시 잠재 상태로 되돌른다.

4. Compressor Distortion Ratio コンプレッサ率
4-1. Connect a 150mVpp, 400Hz, 0-4 cycle burst signal to the INPUT jack.
4-2. Connect the oscilloscope to the TP-3 (pin 7 of IC3) on the MT board.
4-3. Adjust the RT-2 on the MT board to minimize the DC drift.
4-4. INPUT jack for 400Hz, 150mVpp, P0 = 4-0-4 instinct phase signal to input.
4-5. TP-3 (MT board, IC-3) 0.75Vpp to connect the oscilloscope.
4-6. DC level is the lower limit. MT board, RT-2 (THD) to measure.

5. A/D/A Bias A/D/パネルバイアス
5-1. Connect a +6dBm, 1kHz, sines signal to the INPUT jack.
5-2. Connect the oscilloscope to the TP-4 (pin 1 of IC2) on the SUB board.
5-3. Adjust the RT-4 on the MT board for most symmetrical waveform.
5-4. INPUT jack for 1kHz, 4+6dBm line level input.
5-5. TP-4 (SUB board, IC-2) 0.75Vpp to connect the oscilloscope.
5-6. Waveform line level in 1kHz, 4+6dBm input.

6. Pad Input Offset パッド入力オフセット
6-1. Connect a +10dBm, 1kHz, sines signal to the INPUT jack. Connect an 800mVpp 200Hz, 0-4-0 (0
0-12 cycles) burst signal as shown in Fig. A to the PAD input jack.
6-2. Connect the oscilloscope to the TP-6 (pin 7 of IC3) on the MT board.
6-3. Set the RANGE/MODE knob at the SAMPLER mode.
6-4. Rotate the RT-4 on the SUB board FCW when viewed from component side. Now rotate it CW slowly until the amplitude becomes 200mVpp. Do not advance the RT-2 for a further low
6-5. INPUT jack for 1kHz, 10mVpp signal. Pad input level 0Vpp = 0.75Vpp to connect the oscilloscope.
6-6. TP-4 (MT board, IC-3) 0.75Vpp to connect the oscilloscope.
6-7. RANGE/MODE to SAMPLE-NAME to set.
6-8. MT board, RT-4 to 0Vpp, line level in normal condition.

7. Dynamic DC Offset ダイナミックDCオフセット
7-1. Connect a 150mVpp, 400Hz, 0-4-0 burst signal to the PITCH (KEYBOARD) jack.
7-2. Connect the oscilloscope to the TP-6 (pin 7 of IC3) on the MT board.
7-3. Set the RANGE/MODE knob at the SAMPLER mode (B).
7-4. Adjust the RT-5 on the MT board for minimum DC drift.
7-5. INPUT jack for 400Hz, 150mVpp, P0 = 4-0-4 instinct phase signal to input.
7-6. TP-5 (MT board, IC-3) 0.75Vpp to connect the oscilloscope.
7-7. RANGE/MODE to SAMPLE-NAME to set.
7-8. MT board, RT-5 to 0Vpp, line level in normal condition.

8. Dynamic Bias ダイナミックバイアス
8-1. Connect a +10dBm, 1kHz, sines signal to the INPUT jack.
8-2. Connect the oscilloscope to the TP-6 (pin 7 of IC3) on the MT board.
8-3. Set the RANGE/MODE knob at the DELAY mode.
8-4. Adjust RT-4 on the MT board for 1.5Vpp.
8-5. INPUT jack for 1kHz, 0-10mVpp level input.
8-6. TP-5 (MT board, IC-3) 0.75Vpp to connect the oscilloscope.
8-7. RANGE/MODE to SAMPLE-NAME to set.
8-8. MT board, RT-4 to 0Vpp, line level in normal condition.

9. Expander Distortion Ratio エクスパンダ率
9-1. Connect a 150mVpp, 400Hz, 0-4-0 burst signal to the INPUT jack.
9-2. Connect the oscilloscope to the TP-6 (pin 10 of IC3) on the MT board.
9-3. Set the RANGE/MODE at the DELAY mode.
9-4. Adjust the RT-3 on the MT board for most straight DC line.
9-5. INPUT jack for 400Hz, 15mVpp, P0 = 4-0-4 instinct phase signal to input.
9-6. TP-3 (MT board, IC-3) 0.75Vpp to connect the oscilloscope.
9-7. RANGE/MODE to SAMPLE-NAME to set.
9-8. DC level is the lower limit. MT board, RT-3 (THD) to measure.

Waveform of \( f \) from DB-33