**CSQ-100 SERVICE NOTES**

*First Edition*

Memory capacity — Up to 168 notes (84 notes/channel) 2 channels

- CV output: 1V/oct: -2V to +8V
- CV input: 1V/oct: 0V to +5V
- Gate output: Off: OV On: +15V
- Gate input: Off: OV On: +15V (threshold +2.5V)
- EXT Start input: With switch: normally close, open to start or pulse: +15V
- EXT Step input: +15V pulse

Power consumption: 8 watts

Dimensions: 345W x 305D x 95H mm (13.6 x 12.0 x 3.7 in)

Weight: 2.7 kg (5.94 lbs)

**Panel REMOVAL SCREWS:**

1. Panel H49 (072H049)
2. Switches SLB-623-18F (001-201)
3. Button no.8 (016-008)
4. Screws 3x20mm truss Br
5. Screws 3x6mm Fe Br (11 places)
7. Switch SSBO23-12PN (001-187)
8. Switches w/button SCK41168 (001-275)

**Switches SLE-622-18P (001-268)**

- Rubber bushings no.20 (068-020)
- Side blocks (R L set) H21 (066H021)
- Screws 1 2 3 4
  - 3x10mm Fe Br
  - Tape-tight binding head

**Switches w/button SCK41167 (001-276)**

- Knob no.57 (016-057)
- Pot. VM1O8K20R16 (020-766)
- Knob no.33 (016-033)
- Pot. RWALOP015A26 (029-577)

**Screws**

- 3x6mm Bl Fe Br tap-tight binding head
- Rubber bases G-5 (111-021)
- Rubber bases G-7 (111-023)

**Power transformer**

- 022H024C 100/117V
- 022H024D 220/240V

**Power supply board**

- PSH39 100V
- PSH40 117V
- PSH41 220/240V

**Jacks S37622 (009-012)**

**Screws**

- 3x12mm Fe Br tap-tight B binding head
- 3x10mm Fe Br (8 pcs) tap-tight B binding head

**Roland**

Printed in Japan Nov. '82 E-2 1
### μPD8048 Pin Description

<table>
<thead>
<tr>
<th>Designation</th>
<th>Pin No.</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (Data bus)</td>
<td>1-13</td>
<td>Switch scanning</td>
</tr>
<tr>
<td>2 8</td>
<td>14</td>
<td>CV data</td>
</tr>
<tr>
<td>3 8</td>
<td>15</td>
<td>CV and GATE data</td>
</tr>
<tr>
<td>4 8</td>
<td>16</td>
<td>Address</td>
</tr>
<tr>
<td>5 8</td>
<td>17</td>
<td>RAM address during RAM address scanning</td>
</tr>
<tr>
<td>6 8</td>
<td>18</td>
<td>Output Gate signal</td>
</tr>
<tr>
<td>7 8</td>
<td>19</td>
<td>LED</td>
</tr>
</tbody>
</table>

#### P1 (Port 1)
- 11, 26: RAM address
- 12, 29: RAM address
- 13, 31: RAM address
- 14, 33: Output CV D/H and Gate hold timing
- 15, 35: NTRONIC pulse
- 16, 32: Read switches status during switch scanning
- 17, 34: Select switches status during switch scanning
- 21: GATE input
- 22: CV 16 by-pass enable during the STOP node
- 23: CV 16 bypass enable during the STOP node
- 24: CV 16 bypass enable during the STOP node
- 25, 36: Select switches status during switch scanning
- 26, 37: Select switches status during switch scanning
- 27, 38: Select switches status during switch scanning

#### P2 (Port 2)
- 4: Input to reset the 8048 when power is on
- 5: External gate input
- 6: Digital data input where A-B conversion
- 7: Digital data input where A-B conversion
- 8: Input to reset the 8048 when power is on
- 9: External source inputs for internal oscillator
- 10: External source inputs for internal oscillator
- 11: External source inputs for internal oscillator
- 12: External source inputs for internal oscillator
- 13: External source inputs for internal oscillator
- 14: External source inputs for internal oscillator
- 15: External source inputs for internal oscillator
- 16: External source inputs for internal oscillator
- 17: External source inputs for internal oscillator
- 18: External source inputs for internal oscillator
- 19: External source inputs for internal oscillator
- 20: External source inputs for internal oscillator

#### (Top View)
- 1: Reset input
- 2: XTAL 1 input
- 3: XTAL 1 output
- 4: Reset output
- 5: Select output
- 6: Digit output
- 7: Digit output
- 8: Digit output
- 9: Power input
- 10: Power input
- 11: Power input
- 12: Power input
- 13: Power input
- 14: Power input
- 15: Power input
- 16: Power input
- 17: Power input
- 18: Power input

**Note:**
The μPD8048 is an 8-bit parallel computer fabricated on a single silicon chip. The 8048 contains a 1k x 8 ROM program memory, 27 I/O lines, an 8-bit timer/counter and clock circuits.

Used in the CSQ-100 is a μPD8048-02B version in which program and data dedicated to the CSQ-100 are stored in the program memory.
CIRCUIT DESCRIPTION

This description is divided into parts: the general description which explains roughly the functions of CSQ-100, and the detailed description which centers around A/D and D/A converters since these are practically the heart in this instrument. Complete understanding of A/D and D/A conversion circuits will aid in performing adjustments in Section II.

Function of "One chip computer" uPD8048
CSQ-100 performs its functions with uPD-8048 at the center position for all, including the following in its performance cycles:

1. Switch Scanning
2. D/A Conversion
3. A/D Conversion
4. Write/Read of Data to or from External RAM
5. Timing for lighting LED Indicator
6. Triggering of METRONOME
7. Holding of GATE OUT
The D/A converter transforms the sequential data (switch scanning, RAM address, CVs, etc.) which are being output from the 8048 through internal programming, into analog voltages. Since the D/A converter (DAC) employed here is a summing type, with a weight-resistor-tree connected to an inverting input of an OP amp, each bit in the digital data is converted to an analog voltage in value to double the one immediately subordinate to each. When CV data are on output, pulses synchronized to CV data are supplied from P15 of Port 1 onto the Sample and Hold (S/H) circuit, and the analog CV voltage equivalent to the data are held on C124. (Details discussed later)

3. A/D CONVERSION (Analog to Digital)

Since the CV IN is an analog voltage, it must be converted to digital data for making the storing in RAM possible. The method employed in the CSQ-100 is called "successive approximation conversion" where each bit, from DB6 (for MSB; most significant bit) to DB0 (for LSB; least significant bit), is being set successively to output "1" which, after being D/A converted, is to be compared with CV IN at the comparator (311). The comparator will then output "0" (low) if CV VDC, or "1" (high) if CV VDC, onto TO. When H is output to TO, the corresponding digital data is "reset" and becomes 0. Such set and "reset" is repeated 7 times for bits from DB6 to DB0 and with the resultant value from such "set" "reset" the digital data of the CV IN is produced.
4. DATA (CV and GATE TIME) WRITE/READ to RAM

In the external RAM, memory cells are selected by the signal made in combination of the address signals latched on 74LS273 by the instruction signal from ALE (Address Latch Enable) and those from P11 and P13. The data (CV and GATE TIME) are written when WR is "low" and are read when it is "high". Although the data are in 8-bit format, they are written/read in two times separated to one-word-4-bit groups of lower and higher bits.

The pulses are synchronized with those of TEMPO CLOCK GENERATOR and are output at the time rate one pulse for every eight CLOCK pulses. Because of this, lighting on/off cycling rate is also changed along with change in TEMPO, but the current amount to LED is still being kept unchanged through a means to maintain the duty ratio constant.

5. GATE HOLD

From DB7, the GATE signals are also being output. They are held by the signal (the same as for S/H) to become output of GATE signal.

6. LIGHTING of LEDs

Signals for lighting LEDs (except TEMPO) are supplied from DB. However, because there are many signals on DB at every instance, timing pulses are given from P14 to control the LED circuits being fed only when there are output lighting signals.

7. METRONOME DRIVE

In LOAD mode, two pulses synchronized to TEMPO are being output (in period 480 times the CLOCK pulse, in pulse widths of 14μs and 360μs for alternate output). METRONOME amp is driven by both pulses but since the shorter pulses of 14μs are filtered out by the integration circuit of R147 and C115 before arriving at LED, the longer pulses of 360μs only are used for lighting the TEMPO LED.
LOAD

1. Input CV
   -2V -1V 0V 1V 2V 3V 4V 5V 6V 7V
   Ex. 1V

2. A/D (CVD 1)
   36

3. CVD1-24 (CVD 2)
   Store DATA
   Ex. CVD2=12
   12
   (Decimal number)

4. CVD2+24 (CVD 1)
   12+24 =36

5. D/A
   36
   1V

6. Output CV
   LOAD/KCV ADD OFF
   PLAY (KCV ADD ON)

PLAY

Note:
The digital data in this manual are expressed in Decimals.

Read RAM

KCV ADD?

ON

OFF

ADD ON

4. CVD2 + 24

Input CV
being pressed

A/D (CVD 3)

CVD3-24 (CVD 4)

CVD2+CVD4

5. D/A

Output CV
DESCRIPTION OF CIRCUIT FUNCTION

Since in the CSQ-100, the key voltage which are analog quantum are first converted to digital for storing in RAM and again afterward are converted to analog for CV OUT, these A/D and D/A conversions are just as important as the heart is to man. It might be said that without understanding of these conversion principles and pertinent analog vs digital data relationship, all adjustment services which are related to key voltage circuits become difficult to perform correctly.

With this in mind, our description will proceed along with the lines numbered in the figure on the left page.

1. In the CSQ-100, the CV storage range runs from 0V to +5V, or 61 notes.
2. Due to the reason to be touched on later, the lowest CV which is provided by this CSQ-100 is -2V. Therefore the digital data are made to correspond to 00 = -2V.
3. The voltages that can be stored in RAM are 0 to -5V, which makes the number of pitches to be 61 if taken in the ratio of 1V/oct. Although, in handling them, 6 bits (2^6 = 64) are enough, 7 bits would become necessary for the key voltage on the upper range if started from 0V = 24. For this reason, numbers 24 are being subtracted after conversion to digital form to make 0V = 00.(in decimal) The key voltage to correspond to the digital value "1" is about 83.3mV.
4. Reproduction of CV in Memory ------- 1
   - LOAD or PLAY (with KCV ADD "off"

In this case, when D/A conversion is done after addition of 24, which is the same as subtracted before storing, into the data of RAM, the same digital analog voltage can be reproduced after D/A conversion.

5. Reproduction of CV in Memory ------- 2
   - Transpose under PLAY mode, with KCV ADD "on"

CSQ-100 has the function to have a desired transposition of notes in PLAY mode by adding an external key voltage to the CV in memory. But, if transposition is required up or down, KCV must be varied also up or down from the center referenced by the key which produces on this mode the same original tones in pitch from the Memory.

Also, because the CSQ-100 has set this shift down range to be within 2V, the key to produce KCV=2V is made the reference key. For instance, when 0V is stored in Memory, pressing a 0V key, the lowest, will produce transposed output voltage -2V.

For this, the following must be true:

Digital data for 0V stored in RAM (CV2 = 00 )
+ KCV digital data of 0V (CV3 = 24 )

= 00 (-2V)

To satisfy the above, " CVD2 + CV3 = 24 = output data"
When MSB is first set on, the signal "1" is output to DB6. When D/A converted, the analog voltage (VDA) here must be 3.333V which, after shifted down by 41mV, becomes 3.392V (VDC). This time VDC goes into noninverting input of the comparator and is compared with CV IN.

In the case shown in figure left, this CV is 5V, so CV IN < VDC bringing the comparator's output to 1 (0), to have DB6 remained as has been set to "1".

Next, DB5 is set to "1". This time the digital data is the sum of DB6 and DB5, and the comparison becomes CV IN < VDC, to output H and to "reset" signal of TO and to have DB5 return to "0".

This kind of comparison is repeated 7 times down to DBO (LSB). The sum of the digital data of the bits remained "unreset", then, is made to be the data of this CV IN, with which the CV IN is stored in the external RAM.

\[ VDC = VDA - 41mV \]

(precisely, 41.7mV, and voltage differences between notes are 83.3mV or 84mV in turn)

Although CV IN is in fact an analog voltage, steps up or down like a staircase wave as the note changes. Therefore, if VDC is shifted down by an amount equal to about one-half of the voltage difference per key (step rate, or resolution), a voltage fluctuation within the resolution value of the comparator does not bring effect on the digital data, as shown in the figure.
CV OUTPUT Variation
LOAD mode with
1 V key being held
down.

Output increases
as VR106 turned
clockwise.

Further turning
VR106.
When VDC overs
1 V a little,
its data
becomes
rewritten.

Fig. 1

RELATIONSHIP BETWEEN CV ADJ (VR106) and CV DATA

In LOAD mode and with the converter that is correctly adjusted,
suppose that we turn VR106 (CV ADJ) slowly clockwise while
holding 1 V key depressed on the keyboard. Then you can observe
VDA (i.e. CV OUT) increases gradually, and likewise VDC
(VDA - 41.7 mV) ascends along the dotted area as shown in Fig. 3.
That is to say, although the digital data is unchanged, the volt-
age for that data is increased. But, still kept on turning VR106
to have VDC overcome 1 V line for the digital data 36 as shown in
Fig. 4, it causes the output of the comparator to be turned to
"H" and the digital data re-written to 35. Fig. 5 shows that state as being adjusted by turning VR106 clockwise to have CV OUT
again to 1.000 V.
Still turning VR106 further will repeat the same as above and to
rewrite to 34.

But, when turned counterclockwise, the data will be rewritten to a larger number each time.

When watching this on a digital voltmeter connected for obser-
vation, the display will be as illustrated in Fig. 2.
Now, suppose that we have turned VR106 a little too far to
have the digital data 35 for CV IN of 1 V (as in Fig. 5).
It is all right and causes no problem as long as we have KCV
ADD turned off, because under these circumstance, any shortage
or excess of voltage could be compensated for by biasing thru
this CV ADJ. potentiometer. But once we have turned KCV ADD
on, the whole matter would become different, to be explained
on next page.
WHEN DIGITAL DATA IS INCORRECT, ERROR WILL BE PRODUCED on CV OUT with KCV ADD "ON"

Taking for instance the case of each having CV IN 1V converted into digital 35 (B and C, table below) in place of 36, we will explain as follows:

Note: The topmost numbers in the table refer to those on page 6.

<table>
<thead>
<tr>
<th>MODE</th>
<th>2</th>
<th>3</th>
<th>4, 5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CVDI</td>
<td>subtraction</td>
<td>CVD2</td>
<td>addition</td>
<td>D/A INPUT</td>
</tr>
<tr>
<td>A</td>
<td>LOAD (normal)</td>
<td>36</td>
<td>24</td>
<td>12</td>
<td>24</td>
</tr>
<tr>
<td>B</td>
<td>KCV ADD &quot;off&quot;</td>
<td>35</td>
<td>24</td>
<td>11</td>
<td>24</td>
</tr>
<tr>
<td>C</td>
<td>KCV ADD &quot;on&quot;</td>
<td>35</td>
<td>24</td>
<td>11</td>
<td>*(CVD-24)</td>
</tr>
</tbody>
</table>

* This is when the 2V key is depressed so as to have the same pitch on CV OUT with CV IN in memory.

Case B is when VR106 is adjusted to reproduce CV OUT of 1V even if in earlier stage the digital data lacks 1. In this case, since the numbers in preceding subtraction, and subsequent addition are both the same (24), the analog amount at the output receives no effect to differ after A-D-A conversions.

In C, however, despite the fact that the KCV (being pressed) is converted to digital data number short of 1, it is added to RAM-stored data after subtracting 24. This means that there is a double shortage, bringing after all the shortage by 2 before D/A conversion prior to CV OUT. Through this D/A once again, 1 out of these 2 can be compensated for by VR105, but there is still remained of 1, which brings lack in pitch of a semitone ("1" in digital data) on tone reproduction. Thus, a maladjustment of VR106 produces a deviation on reproduction when played with KCV ADD "on". Or, it can be said conversely that, through finding such deviation on analog voltage, it is possible to check digital data errors.

WIDTH ADJUSTMENT with VR105

This potentiometer VR105 is for use to correct the gain of IC113 so as to have D/A in proper relation of 1V/oct, that is, when the data changes by 1, CV OUT changes by 83.3mV.

When VR105 is required for readjustment, it may also be necessary to readjust VR106, since turning either VR results in interactions between adjustments, therefore, both VRs need to be adjusted in turn.

Also care must be exercised to avoid an excessive turn of the VRs which will bring difficulty in performing this adjustment.

D/A ADJUSTMENT with VR104

This potentiometer is for the gain adjustment of the D/A amp, and it is in particular for DB6. This DB6 is for the data weighing the most significant bit, so its adjustment is the most critical one and warrants the careful attention. Sources of fluctuation and deviation such as those coming from the preceding stage of IC103, IC104, on impedance or on output voltage, and resistance variation in resistor, etc. are to be compensated for by this VR104.

Since the digital data that makes DB6 active is in number over 64 or 3.333V in CV, fluctuation brought through DB6 data will effect all CV of higher voltages as shown in the figure.

In practice, it will be best to adjust VR104 as follows:

- Set the LOAD mode and complete both CV ADJ and WIDTH ADJ, then, holding down the key for 4V. Set VR104 so that CV OUT equals 4.000V.
Improvement on RESET SENSE

Increasing C104 capacitance from 1 mfd to 10 mfd may make RESET pulse more stable.

Note: 82k is unnecessary when existing C106 is 0.47/50.
Difference between OPH31's:

OPH31D - R212, R213 (100K) are mounted on the component side with the pattern provided.

OPH31B - Both 100Ks are attached on the foil side with pertinent pattern cut.
ADJUSTMENTS

The adjustment is composed of 2 parts: Section I and Section II. It is recommended that the adjustment which is necessitated after the replacement of failing component or others are, as a rule, to be conducted as described in Section I.

Definitions
In this adjustment, the following terms have following meanings,

DVM -------------- Digital Voltmeter
LOAD, PLAY, etc. ------- Key on the CSQ-100 control panel
2V key, 3V key, etc. ----- A key on the synthesizer being used, which provides that KCV
TEMPO, CAL, FAST, etc. --- Control, switch, jack, legend on the CSQ-100 (capital letters)
SCOPE --------------- Oscilloscope
CP1, CP2, etc. ----------- Check point on the PCB.

Note: Before attempting adjustment, warm-up period for no less than 10 minutes should be given.

CAUTION: Care must be taken not to turn the adjusting potentiometers excessively.

SECTION I

Adjustment is usually necessary only after replacing parts.
## Calibration Procedures

<table>
<thead>
<tr>
<th>After replacement of</th>
<th>Connect, Adjust or Check</th>
<th>for</th>
<th>(remark)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC101 (µPD8048) L101 (47µH)</td>
<td>Frequency counter, CP3 L101</td>
<td>365kHz ± 10kHz (8048 Clock frequency)</td>
<td></td>
</tr>
<tr>
<td>IC110 (TC4011P)</td>
<td>Scope, CP4</td>
<td>(waveform check)</td>
<td></td>
</tr>
<tr>
<td>IC111 (TC4049P, D129 (1S259))</td>
<td>Frequency counter, CP2 VR102 Clock Adj.</td>
<td>(Tempo clock frequency) 4.7kHz ± 5% with TEMPO at FAST Check that frequency is 0.7kHz ± 5% - 10% with TEMPO set at SLOW. If this range deviates, readjust VR102 with TEMPO at FAST within the range of 4.7kHz ± 5%. Or, vary the capacitance of C109.</td>
<td></td>
</tr>
<tr>
<td>IC114 (TL080CP)</td>
<td>No connection at CV IN jack CV OUT, DVM VR109 Offset</td>
<td>(Depress RESET) 0 ± 0.5mV</td>
<td></td>
</tr>
<tr>
<td>IC112 (µPD4558) D129 (1S259)</td>
<td>DVM, CP1 VR101 -15V Adj.</td>
<td>-15V ± 2mV</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Since any variation in the DC supplies will have the most pronounced effect on the DA converter, check CV OUT for error through the next steps (6).

| IC103, IC104 (TC4049) IC113 (TL082-P) | CV IN, SYNTH'S CV GATE OUT DVM, CV OUT VR106 CV Adj. | (DA Adj.) CAUTION: Adjustment of the DA converter is very subtle. Always rotate ADJ. pots by slow degrees, excessive turn will bring great difficulty into the subsequent adjustment attempts, requiring a waste of time. |

**Setting:**

- PORTAMENT on the synthesizer ----- Off or minimum
- LOAD MODE -------------------------- CV/GATE
- MEMORY ----------------------------- CH1
- PLAY MODE -------------------------- KCV ADD ON REPEAT
- TEMPO ------------------------------ center
- PORTAMENT ------------------------- 0
- CALIBRATION (knob) ----------------- center
6-1. Press **RESET** and **LOAD**.

6-2. Depress the 2V key, DVM must read 2.000V ± 3mV. When DVM reads within 3mV, adjust CALIBRATION pot for 2V CV OUT with PUSH CAL depressed. Then proceed to 6-3, 6-4. If reading is outside ± 3mV range, set CALIBRATION pot at center, and adjust VR106 (CV Adj.) for 2.000V ± 3mV reading.

6-3. Verification of KOV ADD function

While depressing the 2V key, push **PLAY**. DVM must read the same.

A. If reading changes, it means that VR106 (CV Adj.) has been set at incorrect point. Proceed to Section II

B. When the reading is steady, make sure that DVM readings are within the ranges in the table shown below with respective key depressed. (RESET-LOAD-2V key-PLAY-2V key-3V key-4V key)

<table>
<thead>
<tr>
<th>key being depressed</th>
<th>DVM reading (CV OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2V</td>
<td>2.000V ± 2mV</td>
</tr>
<tr>
<td>3V</td>
<td>3.000 ± 2mV</td>
</tr>
<tr>
<td>4V</td>
<td>4.000V ± 2mV</td>
</tr>
</tbody>
</table>

If any of the readings exists outside the limit, make adjustment under SECTION II, 1-6.

6-4. Press **RESET** and **LOAD**.

While depressing 4V key, press **PLAY**.

DVM must read 6.000V ± 3mV. If not, proceed to SECTION II, 1-7.
SECTION II

1. ADJUSTING DA CONVERTER

Some procedures are the same as described under Section I.
In the following steps, adjustment should be made with specified key being depressed.

1-1. Connection and Settings: Follow the instruction "6" in Section I.
1-2. Press RESET and LOAD.
1-3. While depressing 2V key, adjust VR106 (CV Adj.) for 2.000V reading. Then, press PLAY.
   A. If the reading stays unchanged, proceed to step 1-6.
   B. If it changes, proceed to step 1-4. (note the reading)
1-4. Press RESET, LOAD and 2V key.
   While depressing the 2V key, adjust VR106 for a following "2"V according to the deviation noted at step 1-3,B.
As discussed earlier (RELATIONSHIP, CV ADJ and DATA), DVM reading will repeat the cycle of 2V ± 41mV as VR106 being turned.
Ordinal number in the right column of the table below shows number of repetition.

<table>
<thead>
<tr>
<th>DVM reading at step 1-3,B (approx)</th>
<th>Turn VR106 in this direction</th>
<th>Stop turning when DVM reads 2.000V of</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.083V</td>
<td>clockwise</td>
<td>1st</td>
</tr>
<tr>
<td>2.167V</td>
<td>clockwise</td>
<td>2nd</td>
</tr>
<tr>
<td>2.250V</td>
<td>clockwise</td>
<td>3rd</td>
</tr>
<tr>
<td>1.917V</td>
<td>counterclockwise</td>
<td>1st</td>
</tr>
<tr>
<td>1.833V</td>
<td>counterclockwise</td>
<td>2nd</td>
</tr>
<tr>
<td>1.750V</td>
<td>counterclockwise</td>
<td>3rd</td>
</tr>
</tbody>
</table>

1-5. Press RESET, LOAD, 2V key and PLAY. (2V key held down)
DVM must keep the same reading.
1-6. Press RESET and LOAD.

<table>
<thead>
<tr>
<th>key to be pressed</th>
<th>adjust</th>
<th>for reading</th>
<th>repeat until DVM reads</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-61</td>
<td>3V</td>
<td>VR105(WIDTH)</td>
<td>3.000V</td>
</tr>
<tr>
<td>1-62</td>
<td>2V</td>
<td>VR106(CV Adj)</td>
<td>2.000V</td>
</tr>
<tr>
<td>1-63</td>
<td>4V</td>
<td>VR104(AD Adj)</td>
<td>4.000V</td>
</tr>
<tr>
<td>1-64</td>
<td>2V</td>
<td>VR106</td>
<td>2.000V</td>
</tr>
<tr>
<td>1-65</td>
<td>3V</td>
<td>VR105</td>
<td>3.000V</td>
</tr>
</tbody>
</table>

repeat until respective voltages are displayed on DVM
1-7. Press **RESET**, **LOAD**, 4V key (holding down) and **PLAY**. DVM should read $6.000V \pm 2mV$.

1-8. If DVM proves that deviation is outside this range, it may be cured by turning VR105, but this adjustment will affect steps 1-64, 1-65. Turn VR105 within the limit of $2.000V \pm 2mV$ and $3.000V \pm 2mV$.

2. **CHECKING CV OUT**

   With DVM connected to CV OUT and **LOAD** pressed.

   Check the DVM readings for 1V/oct through entire keyboard.

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**Note:** When difficulties arise in relation to WIDTH and CV adjustment, VR104, VR105 and/or VR106 might have been set too far from their proper position. Reset them to the approximate positions illustrated in figure right. Adjust again from appropriate step.
<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>072H049</td>
<td>Panel H49</td>
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<tr>
<td>066H021</td>
<td>Side block H21 set of L and R</td>
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<tr>
<td>061H080</td>
<td>Chassis H80</td>
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<tr>
<td>068-020</td>
<td>Bushing no. 20 panel</td>
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<tr>
<td>111-021</td>
<td>Rubber Foot G-5 rear</td>
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<tr>
<td>111-023</td>
<td>Rubber Foot G-7 front</td>
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<tr>
<td>016-008</td>
<td>Button no. 8 gray power switch</td>
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<tr>
<td>016-057</td>
<td>Knob no. 57 TEMPO</td>
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<tr>
<td>016-033</td>
<td>Knob no. 33 PORTAMENTO</td>
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<tr>
<td>063-012</td>
<td>Strip no. 12 knob no. 33</td>
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</table>

**POWER TRANSFORMERS**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>022H024C</td>
<td>100V/117V</td>
<td></td>
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</tr>
<tr>
<td>022H024D</td>
<td>220V/240V</td>
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<tr>
<td>022-136</td>
<td>Coil 24M-067-033 47µH</td>
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<tr>
<td>009-012</td>
<td>Jack S37622 no. 8 mono</td>
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<tr>
<td>068-018</td>
<td>Bushing no. 18 red jack</td>
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<tr>
<td>068-005</td>
<td>Bushing no. 5 jack</td>
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<tr>
<td>121-005</td>
<td>Washer no. 5 jack</td>
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</table>

**FUSES**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>008-040</td>
<td>MGP 0.500 CSA prim 117V</td>
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<tr>
<td>008-061</td>
<td>SEMKO T315mA prim.</td>
<td>220/240V</td>
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<tr>
<td>008-056</td>
<td>SEMKO T100mA sec.</td>
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<tr>
<td>008-066</td>
<td>SEMKO T1A sec.</td>
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<tr>
<td>012-003</td>
<td>Fuse clip TF758</td>
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</table>

**SWITCHES**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>001-215</td>
<td>SDG5P 001-1 power 100V</td>
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<tr>
<td>001-216</td>
<td>SDG5P 001-2 power 117V</td>
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<tr>
<td>001-217</td>
<td>SDG5P 502 power 220/240V</td>
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<tr>
<td>001-068</td>
<td>SLE-622-18PS lever</td>
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<tr>
<td>001-201</td>
<td>SLE-623-18PS lever</td>
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<tr>
<td>001-183</td>
<td>SSB-023-12PN slide</td>
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<tr>
<td>001-276</td>
<td>SCK41167 key</td>
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<tr>
<td>001-275</td>
<td>SCK41168 key</td>
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**PCBS**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>149H031D</td>
<td>OPH31D (052H171D-1)</td>
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<tr>
<td>149H070D</td>
<td>OPH70D (052H171D-2)</td>
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<tr>
<td>146H039A</td>
<td>PSH39A (052H172A) 100V</td>
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<tr>
<td>146H040A</td>
<td>PSH40A (052H172A) 117V</td>
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<tr>
<td>146H041A</td>
<td>PSH41A (052H172A) 220/240V</td>
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<tr>
<td>048H017</td>
<td>Heat sink H17 PSH-</td>
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<tr>
<td>042-039</td>
<td>Check point 59B38806</td>
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**POTENTIOMETERS**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>029-577</td>
<td>EVALOPC15A26 2MA slide PORTAMENTO</td>
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<tr>
<td>030-951</td>
<td>EVHLWAD25B15 100KB CALIBRATION</td>
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<tr>
<td>028-766</td>
<td>VM10RK20B16 1MB TEMPO</td>
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<tr>
<td>030-465</td>
<td>SR19R 10KB trimmer</td>
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<tr>
<td>030-471</td>
<td>SR19R 100KB trimmer</td>
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<tr>
<td>030-644</td>
<td>RJ-6P 500B trimmer</td>
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<tr>
<td>030-645</td>
<td>RJ-6P 1KB trimmer</td>
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<tr>
<td>030-646</td>
<td>RJ-6P 50KB trimmer</td>
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**RESISTORS**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>044-927</td>
<td>CRA1BY 11K 0.1% 50PPM</td>
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<tr>
<td>044-932</td>
<td>CRA1BY 31K 0.1% 50PPM</td>
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<tr>
<td>044-929</td>
<td>CRA1BY 125K 0.1% 50PPM</td>
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<tr>
<td>044-930</td>
<td>CRA1BY 250K 0.1% 50PPM</td>
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<tr>
<td>044-972</td>
<td>CRA1DY 500K 0.5% 50PPM</td>
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<tr>
<td>044-973</td>
<td>CRA1DY 1M 0.5% 50PPM</td>
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<tr>
<td>044-838</td>
<td>CRB4FX 10K 1%</td>
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<tr>
<td>044-846</td>
<td>CRB4FX 100K 1%</td>
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<tr>
<td>044-860</td>
<td>CRA1FX 1M 1%</td>
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</tbody>
</table>

**CAPACITOR**

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Description</th>
<th>Model</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>037-035</td>
<td>Disk ceramic 0.1 mfd +80% 12V</td>
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<tr>
<td></td>
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<td>-20%</td>
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</table>
SEMICONDUCTORS

LSIs

179-028 μPD8048C-028
8-bit microcomputer
or μPD8048C-077

can be interchanged

020-202 μPD2114LC RAM

ICS

020-203 SN74LS00N
020-204 SN74LS273N
020-120 SN74LS06N
020-040 TC4011BP
020-075 TC4049BP
020-199 μPC311C
020-100 TL082CP
020-200 TL080CP
020-097 μPC4558C
020-205 μPC14305 +5V regulator
020-206 μPC78L15 +15V regulator

TRANSISTORS

017-016 2SK30A-GR FET
017-106 2SC1815-GR
017-024 2SA733-P
017-034 2SA682-Y

DIODES

018-014 1S2473
018-097 1S259 zener temperature compensated
018-089 1B4B41 rectifier stack
018- 1B4B1 rectifier stack

LEDs

019-028 TLR-124 red
019-029 TLG-124 green
019-009 LR0601R red

WAFFER TERMINALS, TERMINAL, WIRING ASSEMBLIES

010-195 Terminal 5046-05A
010-196 Terminal 5046-07A
042-032 Terminal TT 501-D01 line cable
053H046 Wiring Assy A
053H047 Wiring Assy B
053H048 Wiring Assy C

MISCELLANEOUS

065H050 Dust cover H50
120-001 Long nut no.1 3x10mm
120-003 Long nut no.3 3x18mm
(stand-off or spacer)
012-043 IC Socket
ICC030-040-350T
(μPD8048)
064H076 Holder H76
064H055A Holder H55A
064H083 Holder H83

Commonly available parts:
Resistors of 1/4W, 5%, Mylars,
Electrolytics are omitted.