JUPITER-8

JP-8 SERVICE NOTES

Second Edition
December, 1982

This Notes makes First Edition obsolete and consists of two parts:

Part 1  Previous First Edition .... pp.1–31
Part 2  Mainly applicable to JP-8 units with Serial Numbers
        171700 and above .... pp.32–46
Parts List Change .... p.47
Appendix .... pp.48–50

BEFORE READING
PLEASE CHECK FOR CHANGE INFORMATION
AND CONTENTS AT PAGES 32 AND 33
OF THIS NOTES.

SPECIFICATIONS

- Keyboard: 61 Note, 5 Octaves
- VCO
- VCO 2 Fine Tune Range: ±50 Cents
- Gf
- ENV
- ATTACK Time: 1ms – 5s
- Decay Time: 1ms – 10s
- Release Time: 1ms – 10s
- LFO
- Rate: 0.05 – 40Hz
- Delay Time: 0 – 4ms
- Master Tuneable Range: ±500Hz

Arpeggio
- Rate: 1 – 20Hz
- Audio Outputs
- Upper: 0dBm, 50 Ohm, Balanced
- Lower: 0dBm, 50 Ohm, Unbalanced
- Highest Output CV: 0 – 5V
- Gate: OFF – 0V, On – ±5V
- Dimensions: 100(W) x 485(D) x 120(H)mm
- Weight: 22kg
- Power Consumption: 90W

JP-8 PANEL PARTS LIST

1. Pot. GM70R-K20854 (50KB x 2) (13219812)
2. Pot. GM70R-K20AC54 (50KA, C) (13219811)
3. Pot. LFE9R-C16A55 (50KA) (13339414)
4. Switch SRM1034-K15 (13119301)
5. Switch SLE622-18PS (13139137)
6. Pot. VM10R-K20B814 (10KB) (13219225)
7. Pot. LFE9R-C16B14 (10KB) (13339415)
8. Switch SOPR-24-12P (13159603)
9. Pot. LFE9R-C16B54 (50KB) (13339413)
10. Pot. MFE9R-C16B54 (50KB x 2) (13359302)
11. Pot. VM10R-K20A55 (50KA) (13219231)
12. Pot. VM10R-K20C54 (50KC) (13219243)
13. Switch SLE623-18P (13139135)
14. Switch w/key top KEH10003 (13129717)
   See Parts List for Key top and Switch
15. Bender assy PB-4 (029-022)
16. Cover H80 (065H080)
    LED LNS268A (15029404)
17. Switch KHC11901 (13169601)

Buttons
- No.1, 38  RED (016H018)
- No.2, 5, 34-37  ORANGE (016H012)
- No.6, 9, 30, 33  YELLOW (016H017)
- No.10, 13, 21, 28  WHITE (016H010)
- No.14, 15, 29  GREEN (016H014)
- No.16, 18, 39, 41  BLUE (016H013)
- No.19, 20  DARK BLUE (016H011)

18. Pot. VM10A-K15854 (50KB CT) (13229131)
19. Switch SLE-622-18P (13139128)

All rotary knobs No.88 (016-078)
All slider knobs H4 (016H004)
DISASSEMBLY
Remove screws 1, 2 and 3.

NOTE:
Preparation of a stay and a prop is recommended for a stable top panel rest.

PRECAUTIONS
1. Do not pinch flat cables in the pcbs when closing panel assemblies. Prongs on PCBs will pierce humped cable, causing circuits to malfunction. Stretch rolling cable out.
2. Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, PCBs are temperature-sensitive.
**WIRING DATA TABLE**

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<thead>
<tr>
<th>CONNECTOR</th>
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<td>TUNE VR</td>
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CPU BOARD OPH121(149H121) (pcb 052H267)

Refer to Page 38 for:

CPU CHANGE INFORMATION
CAUTIONS ON  MODULE CONTROLLER BOARD REPLACEMENT
RAM (MOD CON BOARD) REPLACEMENT
CPU BOARD WILL BE AFFECTED BY THESE REPLACEMENTS
MODULE CONTROLLER

OPH123(149H123) (pcb 052H269)

SN 090600-192099

REFER TO PAGES
49–50 for SN up to 090599
36–37 for SN 202100 up
37–38 for PCB or RAM REPLACEMENT
MODULE BOARD
OPH124(149H124)
(pcb 052H270)

SEE PAGE 48
For SN up to 090599

- R256
- Selected on slow rate
- TLO8C Apcs
- Carbon R25
- Metal film R25
- MPS-536-036661
- Proc-SP102
- 2SC155-2R
- 2SC815-2R
- 2SC155-1R
- 2SK301-2R
- NP510
- 152473
- BA662
- 8T-6P

- A or B
- selected on VTR (gm)
- replacement should be
- of the existing

- Selected on offset
- 10 ppm
- with set

- SR2
- base point LC-25
- (16.0 ohm)
- polystyrene film
- bipolar
See pp. 34–35 for SN171700 and up

CAUTION

When replacing Interface board bearing edition no. 052H268 (and below) with PCB of 052H268 (and above), refer to pp. 34 and 35 for PROMs versions of CPU board.
PANEL BOARD A  OPH125(149H125) (pcb 052H271)

Component side

Foil side
This is an 8-bit parallel CPU and is compatible with 280 and 68000.

- Instruction set: 150
- Instruction cycle: 1.5ms (4.0MHz)
- Internal registers: 17
- Address bus: 16 bit
- Data bus: 8 bit

**PIN FUNCTIONS**

**ADDRESS BUS** Transfers 14 bits to memory address decoders (CPU board 17, 22 and 25) for controlling the following:
- CPU board - ROM, CMOS, RAM, 8-bit, RAM, Tape, and TTY reading.
- NMI board - RAM, TTY, 10 and VCO select.
Lower 8 bits are transferred to I/O address decoder (interface board - I21, I3, I4 and I6) for controlling the following:
- IN = Function keys, Digital IN (1, 2 and 3), Kay IN, 80/60, CMY - Set 120, Key LED, Matrix, doing sel, key out, 3/4 Up/I, ESC sel, Gate out, INT synch, TTY.

**DATA BUS** Used to transfer 8-bit instructions and data between CPU and memories or I/O device.

- Clock wave: 4 MHz. Derived from 5-kHz oscillator's 8,000,000 cycles/turn through frequency divider.

**REQ** (Memory Request) Indicates that address bus holds a valid memory address for a memory read and memory write.

**IE** (I/O Request) Indicates the presence of an I/O device number at pins 6A-6F during I/O write/read cycle.

**RD** (Memory read) Indicates that CPU wants to read data from memory or I/O device. The addressed memory or I/O device outputs data onto the CPU data bus at positive transition of RD.

**WR** (Memory write) Indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device which takes the data off of the bus at positive transition of WR.

**INT** (Interrupt Request) Whenever INT (J, frequency divided by 2) is fed to CPU every time 120kHz it accepts INT upon finishing processing job then starts executing INT subroutine. When INT acknowledgment is sent INT remains in NL cycle.

**WAIT** Lengths read or write cycle until data on the data bus becomes valid during the presence of memory access signal for timing CPU access time to memory or I/O device.

**SRQ** Initiates CPU circuits upon power on for the 120kHz or when DC voltages drop below specified value.

**SOURCE REGISTER** 16

**DATA BUS** 16

**ADDRESS BUS** 16

**GENERAL PURPOSE REGISTERS** 16

**DECIMAL COUNTER** 8

**BINARY COUNTER** 8

**BUSY COUNTER** 8

**8 BIT MICROPROCESSOR**

**registers**

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</table>
ADJUSTMENTS

DISASSEMBLY
Follow procedure on page 2. Preparation of a STAY (chain or string) and prop is advisable for a stable top panel rest.

PRECAUTIONS
Do not expose your workbench directly to fans, heaters, air-conditioners, etc. especially after disassembling, most circuits are temperature-sensitive.

The adjustments on the JP-8 should not be done more than necessary. Adjustments merely attempted on a particular module (VOICE) might cause sound balance away from entire VOICES and can, in an extreme case, require the same procedures to be done fifteen times for the remainder.

DESIGNATION – TEST POINT, TRIMMER, PCB –
For PCBs that are identical in circuit configuration, most adjustment steps, test points and trimmers do not refer to a particular PCB or module (VOICE), they may be read as ones on a PCB to be adjusted.

MODULE BOARD CD
MODULE C (VOICE A)  
MODULE D (VOICE B)  
MODULE G (VOICE A)  
MODULE H (VOICE B)  
MODULE BOARD GH
MODULE BOARD AB
MODULE A (VOICE A)  
MODULE B (VOICE B)  
MODULE E (VOICE A)  
MODULE F (VOICE B)  

Four module boards, each consisting of two voices, are identical in all aspects, having the same designators with A or B suffix for the same components of two VOICES, e.g. VR1A (VOICE A) and VR1B (VOICE B). Note that each voice contains two VCOs, VCO-1 and VCO-2.

ADJUSTING ORDER
The adjustments proceed from paragraph 1, DC Supply assuming that the JP-8 is completely unadjusted. When adjusting a specific section, begin with lower numbered para. in the relative adjustment section, e.g. first No. 7 BAL, then, No. 8 DEPTH, as directed.

TEST MODES
Adjustments on the JP-8 proceed in TEST MODES. Although three TEST MODES are available for the adjustments, TEST MODE (3) is chosen in this manual unless otherwise specified. (For more details refer to TEST MODE in Circuit Description — separate copy.)

SW-1, LED switch, in close position, allows LEDs (TEST LED) located right to it to be energized regardless of MODE (NORMAL or TEST), when gate signals are fed to them individually. The LEDs function as assignment indicator just as Patch Number LEDs do. Test LEDs find extended application for learning and checking the assignments varying to MODES (KEY, PANEL and ASSIGN) in Normal mode.

* Among key assignments, POLY-1 only changes assigning order — tapping single key (same key) will assign modules from A to H one by one, repeating the order. This is convenient in comparing 8 modules sounds (timbre, pitch, etc.) sequentially at a note.

* Computer provides FSK adjustment (para. 28) program and outputs test signal at SAVE (DUMP) jack when VERIFY is pressed.

* Integrated PATCH NUMBER LEDs serve as module (VCO) indicator for visible checking, identifying VCO(s) being directed by key(s) has been depressed or being held down.

Below confines description to the point inessential necessary for performing the adjustments.

To put the JP-8 into TEST MODE 3
See figure above 3. With power off, throw SW-1-2 on Interface board from OPEN to TEST-1 or -2 (on some early models the switch is oriented opposite, so are labels TEST-1/2 on PCB, left hand one is always SW-1-2 and OPEN position is at label “OPEN” on the SW).

In the TEST MODE 3
The JP-8 has the following functions that are different from those in NORMAL MODE:
All VCOs are uncompensated, i.e. their pitches are left deviated slightly until “TUNE” is pressed.

FOR SATISFACTORY SERVICE WORK
1. Dump user’s preset memory on tape before attempting adjustments and troubleshooting.

2. If TUNE was pressed in previous adjustments, be sure to power off and on the JP-8 before making adjustment which must be done without compu-tune.

3. Plural keying and miscoring will disorder key assignment sequence. Push HOLD or ASSIGN MODE to off and again to on, as appropriate, to restore the order. Use monitor amp to detect erroneous key assignmanet that LED does not distinguish.

4. Make a practice of pushing MANUAL after changing PANEL MODE,

5. Restore SW-1-1 and SW-1-2 to OPEN and load back the data on tape before return the unit to the customer.
BEFORE STARTING ADJUSTMENTS
ALLOW AT LEAST 30 MINUTES FOR WARM-UP PERIOD

1. DC SUPPLY
POWER SUPPLY BOARD

1. Connect Digital voltmeter (DVM) to –15V (terminal 9, 10, 11).
2. Adjust VR1 for –15V+10mV reading.
3. +15V should be +15V+500mV.
4. 5V should be 5V+400mV.

2. DC SUPPLY (VDD)
MODULE, MODULE CONTROLLER
See appendixes for adjustment locations and glossary.
MODs A, B, C and D
1. Connect DVM to MOD AB IC1 pin 4 (VDD).
2. Adjust upper CON VR4 for –13V+5mV.
3. IC1 pin 8 should read +13V+200mV.

3. PANEL POTs VOLTAGES
INTERFACE (INT) PANEL BOARD A
See appendixes for locations and glossary.
1. Connect DVM to INT TP-3 or RB3 (10k) lead facing outside. (See Figs. below right.)
2. Depress CANCEL.
3. Turn all the pots on the panel illustrated fully cW or to 10. Incomplete settings result in a fluctuating reading or dips on a screen if observed with scope.
4. Set VR1 (Panel board A) for +5V+2mV.

4. DAC
INTERFACE (INT)
See appendix for glossary.
1. Connect DVM to OUTPUT CV jack.
2. Press KEY MODE WHOLE.
3. Press CD key, adjust VR2 for 0.000V reading.
4. Press CS key, adjust VR1 for 5.000V reading.
5. Check CD-CS keys for scaling, that those voltages are 1V/oct increments ±2mV.

5. VCO MOD BAL
MODULE (MOD)

See appendices for adjustment locations and glossary.
1. Connect DVM to MOD TP-3 or R107 lead.
2. Adjust MOD VR7 for 0.000V reading.

6. VCO TUNE
MODULE (MOD)

See appendices for adjustment locations and glossary.
Compu-tuned VCO needs to be re-calibrated only if it or associated components have been replaced. If a VCO is excessively out of tune right after a compu-tune, first check MOD BAL, para. 5 and KCV OUT (INT terminals IM-1, IM-3, etc.) for voltage. Seconds, isolate possible causes before attempting VCO adjustments.

As is usual with tuning, several instruments may be used for determining frequency. The calibration proceeds by Lissippus figures with A-442 reference fed to scope's horizontal input.

1. Connect scope to MOD TP-4 or R130 lead.
2. Turn SOURCE MIX fully to VCO-1 or 2 accordingly.
3. Press A3 key, adjust trimpot T for 884Hz.
4. Press A1 key, adjust trimpot W for 223Hz.
5. Repeat steps 3-4 until waveforms are stationary on both keys.
7. These trims interact to each other, repeat steps 3-6 until three notes are on the right frequency.

NOTE:
Make sure that the JP-8 is in the test mode without initially compu-tuned upon power on. To ensure this, turn power off and on. Then, push UNISON, etc. See “TEST MODE” on the first page of this section.
7.1. ENV 1 S OFFSET
MODULE CONTROLLER (CON)
Applicable to the PCB equipped with VR8

This adjustment must be followed by para. 7. See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-7.
   Set scope V to 20mV/div.
2. Adjust CON VR9 for 0V reading.

7. VCO ENV MOD BAL
MODULE (MOD)
On JP-8 mounting CON with VR8, this adjustment must follow para. 7.1.

See appendices for adjustment locations and glossary.

1. Push TUNE.
2. Connect scope to MOD TP-4 with A-442 reference to H IN.
3. Press A2 key, adjust MASTER TUNE for still Lisajous.
4. Slide MOD ENV up to 10. Without additional keying, adjust MOD VR8 for still Lisajous. (Frequency is same as in step 3.)

8. VCO ENV MOD DEPTH
MODULE (MOD)
This adjustment must follow para. 7. See appendices for adjustment locations and glossary.

Change from para. 7 setup: ENV-1 S to 10; VCO-1 to 2×; VCO MOD ENV to 0.

The adjustment sets maximum voltage of modulating waveform to the value by which VCO's can be shifted within a 3-octave range.

1. Press A0 key, adjust MASTER TUNE for motionless Lisajous.
2. Set VCO-1 to 16×; VCO MOD ENV to 10. Leaving A0 key open, adjust MOD VR9 for the same waveform as in step 1.

9. VCO CROSS MOD BALANCE (X-MOD)
MODULE (MOD) MODULE CONTROLLER (CON)

This adjustment must be followed by para. 10. See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 with A-442 reference fed to H IN. Place a ground to CON TP-4 or D-20. Push TUNE.
2. Press A2 key, adjust MASTER TUNE for still Lisajous.
3. Leaving A2 key open, set VCO-1 CROSS MOD to 10.
   Adjust MOD VR10 for the same Lisajous displayed in step 2.

10. VCO CROSS MOD DEPTH (X-MOD LEVEL)
MODULE (MOD) MODULE CONTROLLER (CON)

This adjustment must follow para. 9. See appendices for adjustment locations and glossary.

The adjustment sets modulating voltage to the value by which VCO-1 frequency is shifted by 3 octaves when CROSS MOD is set at 5, and VCO-1 RANGE at 2×.

Change from para. 9 setup: VCO-1 CROSS MOD to 5; VCO-2 SYNCH to on; VCO-2 RANGE to LOW FREQ.

1. Press A0 key, adjust MASTER TUNE so that Lisajous is 5×1.
2. Switch VCO-2 WAVE to square; VCO-1 to 16×7. Adjust MOD VR11 to display Lisajous observed in step 1.

11. PULSE WIDTH MOD LEVEL (P.W.M.)
MODULE (MOD)

On JP-8's S/N **06000** and subsequent, waveform is up side down.

See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-4 or R130 lead. Trigger on the negative edge (positive S/N **08000**).
2. Press C2 key, adjust MOD VR12 for 30μs pulse width.

NOTE: VR12's interact to each other. Check other voices for mark/space ratio. Readjust as necessary.
See appendices for adjustment locations and glossary.

1. Connect scope to MOD TP-6.

   CAUTION: On early product, legends for some VR’s are incorrect. Refer to PCB layout in appendix.

2. Press A2 key, adjust VR13 for 10V p-p reading.

13. VCF KEY FOLLOWER

   MODULE (MOD)   MODULE CONTROLLER (MOD CON)

   See appendices for adjustment locations and glossary.

   This adjustment must be followed by para. 14-17.

   CAUTION

       On early product, legends for some VR’s are incorrect. Refer to PCB layout in appendix.

   1. Place ground to CON TP-4 or D30 cathode.
       5. Press C4 key, adjust VR15 to display 4 complete cycles.

       2. Connect scope to MOD TP-6 or R166 lead.
       4. Press C2 key, adjust scope timebase and VCF FREQ to display one complete cycle. (arrow the particulates, same for the rest para.) MOD VR20 may be used for fine adjustment.

       3. Turn MOD VR14 fully clockwise. The VCF’s resonate.

   NOTE: VR14 and VR20 will be readjusted in later para.

14. VCF WIDTH

   MODULE (MOD)   MODULE CONTROLLER (CON)

   Para. 13-17 must be performed in sequence.

   1. With scope to MOD TP-6 set timebase to 1ms (2m/s/div).
   2. Press C2 key, adjust VCF ENV MOD and MOD VR20 to display one complete cycle.

   On JP-8’s S/N **0600 and subsequent, read figures in parentheses.

   3. Set CD FREQ to 10, scope timebase to 5us/div (20us/div). Adjust VR19 to display one complete cycle (5 cycles).

   Steps 2 and 3 interact, repeat steps as required.

15. VCF ENV MOD

   MODULE (MOD)   MODULE CONTROLLER (CON)

   Para. 13-17 must be performed in sequence.

   Change para. 14 setup: VCF ENV MOD to 0, scope timebase to 0.2ms/div.

   1. Press C2 key, adjust CD FREQ and MOD VR20 to display exactly one complete cycle.

   2. Reset VCF ENV MOD to 10, timebase to 50us/div.

   Adjust VR21 to display 16 complete cycles.

16. VCF TUNE

   MODULE (MOD)   MODULE CONTROLLER (CON)

   Para. 13-17 must be performed in sequence.

   Change setup in para. 15 step 2: ENV MODE to 0; CD FREQ to 5 (S/N **0600 – 4); scope to MOD TP-6 with A-442 reference fed to H IN.

   1. Press a key, adjust VR20 for 1:1 Lineout.

17. RESONANCE LEVEL

   MODULE (MOD)

   Para. 13-17 must be performed in sequence.

   Change setup in para. 16: SOURCE MIX to VCO-1; CD FREQ to 10; Scope to INT TRIG.

   1. Press A2 key (S/N **0600 – E3 key), adjust VR14 for the figure:
18. VCA LEVEL

MODULE (MOD)  MODULE CONTROLLER (CON)  (early JP-8)

See appendices for adjustment locations and glossary.

Although CON VR5 is included in part 1, the trimpot is replaced by a 10k resistor on later products.
When adjusting MOD replacement, ignore VR5 trimming, following Part 2.
Connect scope to TP-6 or R106 lead.

PART 1
1. Set MOD VR18 wiper to midpoint.

PART 2

19. VCA BALANCE

MODULE (MOD)  MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.

1. Place ground to CON TP-4 or D20 cathode.
2. Connect scope to MOD TP-6 or R106. Switch scope to DC coupling, vertical range to 20mV/div.
3. While tapping a key, adjust VR17 so that DC variations are minimized.

20. ENVELOPE TOTAL TIME

MODULE (MOD)

See appendices for adjustment locations and glossary.

This adjustment proceeds on the assumption that all VOICEs' ENVs are unadjusted. When adjusting particular module, start from step 3 with scope VIN connected to TP-6 of well calibrated module.

ENV.1
1. Connect scope to MOD GH R183B lead or TP-8B.
2. While holding a key, time Attack period on scope. Adjust MOD H VR22 for 6-sec attack period.
4. Press and hold a key repeatedly, adjust both ENV-1 ATTACK (around 4-5) and timebase VAR1 or vernier so that envelope's falling edge is centered on the screen.
5. Shift V lead to TP-8 of the module to be adjusted. Adjust the VR22 for centered falling edge.

ENV.2

The procedure is similar to those in ENV-1, but connect scope to R189 lead or TP-7 and adjust ENV-2 ATTACK and VR23.
21. LFO MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.

1. Connect scope to CON TP-5 or RS9 lead. Set timebase to 10ms/div.
2. Adjust CON VR5 to display exactly 3 complete cycles on the scope.
3. Adjust CON VR2 for slope straightness as shown in Fig. right.
4. Shift scope to TP-4 of (Upper — MOD A; Lower — MOD E).
   Rearrange holding a key, adjust CON VR8 so that VCO becomes being modulated approx. 4 sec after the key first depressed.

22. VCO LED MODULATION

MODULE (MOD) MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.

1. Connect scope (with A-442 into H IN) to TP4 of (Upper-MOD A; Lower — MOD E).
2. Press A2 key, adjust MASTER TUNE for 1:1 Lissajous.
3. Set VCO LF MOD to 10. Lissajous ratio is now changing up and down in sympathy with LFO rate. Adjust CON VR6 so that Lissajous becomes 2:1 at the highest pitch. Note that LFD modulated VCO swing equals 2 octs.

23. VCF LED MOD LEVEL

MODULE CONTROLLER (CON)

See appendices for adjustment locations and glossary.

1. Connect scope to TP-6 of (Upper — MOD A; Lower — MOD E).
2. Press C2 key (S/N **0000— C4 key), adjust CON VR7 for 50 percentage modulation.

24. NOISE

MODULE CONTROLLER (CON)

NORMAL RANGE LOW FREQ

See appendices for adjustment locations and glossary.

1. Switch VCO 2 RANGE to NORMAL. Connect connect to CON TP-4.
2. Adjust CON VR1 so that dense signal peaks are approx. 5V p-p.
3. Switch RANGE to LOW FREQ, check peaks for clip.

25. BENDER OFFSET

BENDER MODULE (MOD)

JUPITER-8

See appendices for adjustment locations and glossary.

1. Connect scope to TP-4 of (Upper — MOD A; Lower — MOD E) with A-442 reference to H IN.
2. Press A2 key, adjust MASTER TUNE for Lissajous.
3. Set VCO MOD switch to on, adjust VR1 (Upper) or VR2 (Lower) for stationary Lissajous.
   NOTE: On JP-8 S/N **0700—, next comes para. 25-1, BENDER LEVEL.

25-1. BENDER LEVEL

BENDER MODULE (MOD) APPLICABLE S/N with **0700 and SUBSEQUENT

JUPITER-8

VR3 BENDER ADJ

1. Connect scope to TP-4 of any MOD. Press A2 key, adjust timebase and vernier (VAR1) to display one complete cycle.
2. Press A3 key, Sway and hold BENDER Lever at extreme left, adjust VR3 BEND to display 1 cycle.
3. Press A1 key, Sway and hold BENDER at extreme right, set VR3 for complete 1 cycle.

26. FSK

CPU

See appendices for glossary.

1. Join TAPE MEMORY LOAD and DUMP jacks via cable.
   NOTE: DUMP is renamed as SAVE on later products.
2. Connect scope to CPU TP-7.
3. Push VERIFY. Be sure that the JP-8 is in test mode, this is displayed in PATCH NUMBER window as —Independent—.
4. Set CPU VR1 for 50% duty cycle.
5. Push VERIFY again at the end of adjustment.
APPENDIX I
CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS

MODULE CONTROLLER BOARD

APPENDIX II
MODULE BOARD
GLOSSARY
DVM Digital Voltmeter
SCOPE Oscilloscope
CPU CPU Board
MOD Module Board
Module (VOICE)
CON Module Controller Board
INT Interface Board

For accessing to MODs E, F, G, H and lower MOD CON, connectors LM1 and HL on upper MOD CON may be disconnected during the service. Do not remove screws at hinges on upper PCBs for more adjustments of lower PCBs. Remounting is not easy. Before reconnecting, switch power off. Incorrect pin connections cause short circuit ICs.

On early PCBs, legends for VR13, 14, 16 are incorrect. Follow this arrangement.

CIRCLED NUMBERS AROUND PCB LAYOUT CORRESPOND TO PARAGRAPH NUMBERS
PART 2

The following pages cover the information of Engineering changes and various aspects of JP-8 affected by the changes.

DESIGNED CHANGES THAT CHANGE FEATURE OF THE JP-8

DAC
To have JP-8 more stable in pitch, DAC for KCVs is changed from 12-bit to 14-bit version.

KEY SPLIT POINT
To make JP-8 more convenient for the user to play on, key split point becomes under the control of the player.

DIGITAL COMMUNICATION INTERFACE OC-8 & DCB
To have JP-8 externally controlled through Digital Data Bus connecting either to digitally operating “musical instrument” or to Analog/Digital Interface Unit (e.g. OP-8 that accepts analog CVs in parallel), Digital Communication Interface Board (DCIB) is built in.

OC-8: First, DCIB is named OC-8 and sold as an optional kit.
DCB: Second, another version of DCIB, called DCB is incorporated in the later JP-8 as a standard feature.

The above-mentioned changes and other significant changes not found on the First Edition of JP-8 Service Notes are listed on the table right.

PARTS LIST CHANGE

APPENDIX

PCB LAYOUTS FOR EARLY 500 JP-8’s
MODULE BOARD
MODULE CONTROLLER BOARD
Not published previously, these drawings will help to trace signal paths on old PCBs.

<table>
<thead>
<tr>
<th>EFFECTIVE SERIAL NUMBER</th>
<th>MAJOR CHANGE</th>
<th>PART INVOLVED</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Below 171700</td>
<td>OC-8 (OPTION): TEST PRODUCTION built into JP-8 with programmable KEY SPLIT feature</td>
<td>PROM Program [CUP board]: IC34--IC36 Version from 1.0 to 2.1</td>
<td>made only on a few JP-8’s see table on the next page</td>
</tr>
<tr>
<td>171700</td>
<td>D/A CONVERTER... from 12-bit to 14-bit format</td>
<td>INTERFACE BOARD: PCB 052H268 to 052H268 DAC (IC14) from Am8012 to ITS80141 Some ICs and circuits CPU BOARD: PROM programs (IC34--IC36) Version 1.0 to 3.1</td>
<td>14-bit INTERFACE BOARD is compatible with the 12-bit pcb only when PROMs of CPU BOARD are replaced with of version 3.1 or 3.2 see P. 34 for detail</td>
</tr>
<tr>
<td>181899</td>
<td>OC-8 (OPTION): made as a commercially available kit for both 12- and 14-bit versions</td>
<td>ROMs IC34--IC36 of CPU BOARD to be replaced upon installing OC-8</td>
<td>IC34--IC36 must be 3.2 version and are supplied in an OC-8 kit together with PROM IC33 containing communication program</td>
</tr>
<tr>
<td>181900</td>
<td>PROMS PROGRAM... revised to be compatible with those stored in OC-8 kit PROMs</td>
<td>CPU BOARD: IC34--IC36 from 3.1 to 3.2 version</td>
<td>additional PROM 3.4D (IC33) only is necessary upon installing OC-8 see table on the next page for detail</td>
</tr>
<tr>
<td>202100</td>
<td>MODULATION CIRCUITS: To have U and L sounds kept balanced</td>
<td>MODULE CONTROLLER BOARD: PCB from 052H269 to 052H269 some circuits</td>
<td>when U or L board is replaced with new one, the remainder should be slightly modified, see pp. 36--38 for detail</td>
</tr>
<tr>
<td>202210</td>
<td>RAM (MODULE CONTROLLER BOARD IC 49): make equivalent RAM usable</td>
<td>CPU BOARD: IC23</td>
<td>short pin 5 of IC23 to ground see p. 38 for modification</td>
</tr>
<tr>
<td>242750</td>
<td>LED DISPLAY: adopt brighter LED</td>
<td>PANEL BOARD F: from LN526RA to LN5620A</td>
<td>new and old LEDs are different in color and brightness mix use should be avoided for uniformity</td>
</tr>
<tr>
<td>272850</td>
<td>FUNCTION SWITCH: LED to diffusive, brighter type</td>
<td>PANEL BOARD E: PANEL BOARD G: function switch from KHCl1901 to KHCl1026 (LED from AR3432S to SEL2210R)</td>
<td></td>
</tr>
<tr>
<td>282680</td>
<td>DCB BOARD (similar to OC-8): built into JP-8 as a standard feature</td>
<td>CPU BOARD MODULE CONTROLLER BOARD PANEL BOARD A</td>
<td>drawings related to this change begin at p. 40</td>
</tr>
</tbody>
</table>
HOW TO IDENTIFY PROM VERSION

CPU BOARD

Version is indicated by hand written number or marking on the label as shown below.
Version can be displayed in PATCH NUMBER window (LOWER). Turn the JP-8 on while pressing PATCH NUMBER buttons 1 and 3.

NOTES:
In 0.7 or 1.0 version, displayed number will change quickly from 07 (10) to 13.
In 3.2 (A, B, C) and 3.3D (3.4) arrangement, number 33 (34) will change to 32 if PROM D is removed.

<table>
<thead>
<tr>
<th>PROM VERSION</th>
<th>PROGRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>12-BIT DAC FIXED KEY SPLIT POINT</td>
</tr>
<tr>
<td>2.0</td>
<td>12-BIT DAC VARIABLE KEY SPLIT POINT</td>
</tr>
<tr>
<td>2.1D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DIGITAL COMMUNICATION INTERFACE</td>
</tr>
<tr>
<td>3.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14-BIT DAC VARIABLE KEY SPLIT POINT</td>
</tr>
<tr>
<td>3.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14-BIT DAC VARIABLE KEY SPLIT POINT</td>
</tr>
<tr>
<td>3.3D (3.4D)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DIGITAL COMMUNICATION INTERFACE</td>
</tr>
</tbody>
</table>

1) This is a special version. Replace each with the same one, or replace all four with a set of 3.2 and 3.4D version.
2) Co-operates with 3.3D or 3.4D for Digital Communication Interface.

When need arises to modify the JP-8 or to replace parts:
First consult the table below, then refer to the right as necessary.

When new feature is required, replace existing part(s) with the one indicated by ●.

Addable new feature  PROM VERSION  INTERFACE BOARD w/14-Bit DAC  by product
<table>
<thead>
<tr>
<th>The JP-8 may be or may have</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Features of the JP-8</td>
<td>PROM A B C D</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>INTERFACE BOARD</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>A B C 3.2 D 3.3 or 3.4</td>
<td></td>
</tr>
<tr>
<td>DAC .......................... 12-bit</td>
<td>DA .................. 14-bit</td>
<td>Variable Split point</td>
<td></td>
</tr>
<tr>
<td>KEY SPLIT POINT .... Fix</td>
<td>SPLIT POINT .... Variable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OC-8 ........................ less</td>
<td>OC-8 ................ built in</td>
<td>Variable Split point</td>
<td></td>
</tr>
<tr>
<td>DAC .......................... 12-bit</td>
<td>DA .................. 14-bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>KEY SPLIT POINT .... Variable</td>
<td>OC-8 ................ built in</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OC-8 ........................ built in</td>
<td>OC-8 ................ built in</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC .......................... 14-bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>KEY SPLIT POINT .... Variable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OC-8 ........................ less</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC .......................... 14-bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>KEY SPLIT POINT .... Variable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OC-8 (DCB) ........................ built in</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

INTERFACE BOARD .................. p. 34
MODULE CONTROLLER BOARD ........ p. 37, 38
RAM IC49 of MOD CON BOARD .......... p. 38
CPU BOARD (in relation to RAM IC49) ... p. 38
OC-8 ........................ OP-8 (OC-8) Service Notes
INTERFACE BOARD OPH122A
(149H122A) (pcb 052H268)
SN 171700 and higher

MAJOR CHANGES
D/A CONVERTER ............ 14BIT
KEY SPLIT POINT ............ PROGRAMMABLE

This board can replace 12-bit INTERFACE BOARD when PROMs of
CPU board are of correct version. See right below.

Besides suffix (A, B, etc.), the PCBs occasionally bear marks "●" and/or "○"
above its code number to show the edition.
● stands for 1, and ○ for 5.
Example: ○●●○ 8th edition

The D/A Converter IC14 is changed from 12-bit Am6012 to 14-bit
IT80141 with this PCB version. Along with the change the following parts
are also changed.

<table>
<thead>
<tr>
<th>PART</th>
<th>From</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latch</td>
<td>LS273 (TTL, IC13)</td>
<td>40H273 (CMOS, IC15)</td>
</tr>
<tr>
<td></td>
<td>LS175 (TTL, IC15)</td>
<td>40H174 (CMOS, IC13)</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>LS175 (TTL, IC11)</td>
<td>40H175 (CMOS)</td>
</tr>
<tr>
<td>Multiplexer</td>
<td>4051 (IC25, IC26)</td>
<td>HD14051 (Hitachi only)</td>
</tr>
<tr>
<td>Flip-flop</td>
<td>74LS74 (IC9)</td>
<td>TC4013</td>
</tr>
<tr>
<td>Gate</td>
<td>LS02 (IC22)</td>
<td>TC4001</td>
</tr>
</tbody>
</table>

Prepare PROMs for CPU board:
A, B, C
3.1 version
or
3.2 version (inevitable when OC-8 exists)
for IC34-IC36

D (when OC-8 is built in)
3.3 or 3.4 version for IC33
Replace existing PROMs with these PROMs.
Adjust DAC circuit, referring to "4. DAC" on p.50 of this book.

NOTES:
This interchange does not affect adjustment procedures except that the
letter "PLL" are displayed in PATCH NUMBER window after 1-1 during FSK adjustment steps.
At the end of Computune cycle(s), defective VCO that has not "tuned-in"
is indicated in MANUAL and PATCH NUMBER or PRESET buttons.
See p.39 for indicators and difference in computuning between 12-bit
and 14-bit systems.
**IMPORTANCE**

When replacing MOD CON BOARD or RAM IC49, SEE PAGE 38 (P.48 for early 500 units).

**CHANGE INFORMATION**

(Each heading is followed by address to the circuit diagram.)

1. **NOISE GENERATOR (D-H, 18-27)**
   
   IC3: from TL082 to BA662 having AGC.  
   NOISE LEVEL VR1: omitted

2. **SAMPLING SIGNAL**
   
   Previous circuit:  
   Only white noise is routed to S/H circuit regardless of VCO-2 RANGE position.  
   New circuit:  
   Pink noise is selected for S/H when RANGE is in LOW position.

3. **D/A CONVERTER (O-R, 23)**
   
   Ladder Resistors: from discrete to resistor array

4. **NOISE KILLER SWITCH (D-E, 28)**
   
   Newly attached for cutting off noise signals.  
   Used in particular adjustments. Close this switch when step states "Place a ground to MOD CON TP-4".

5. **RESONANCE SWITCH (M,33)**
   
   To emphasize regeneration to the point of oscillation. Used for factory adjustment only.

6. **LFO DELAY CONTROL (R, 33)**
   
   From TR25 and TR26 to single paired-transistor TR25 to have U and L delay times synchronize with each other.

7. **LFO RATE (V,33)**
   
   From TR11 and TR12 to single paired-transistor TR11. To minimize speed difference between U and L LFOs.

8. **Add D29 and C95 to +B pin of IC7 (S, 36)**
   
   to stabilize the supply voltage

9. **VCO LEVEL (I, 33-34)**
   
   Apply a ground to pin 5 of IC2 through R21, previously—15V. Change resistors values in this section.

   To set VCO-1 and VCO-2 audio levels to an equal amount when SOURCE MIX is set at 12 o'clock position.  
   To have the same volume changes in VCO-1 and VCO-2 sounds, that is, the change in volume of VCO-1 when SOURCE MIX is being rotated toward VCO-1 is the same as that of VCO-2 when S.M. being toward VCO2.

10. **VCA MOD (Q, 38-39)**
    
    Add C97 across pins 1 and 2 of IC13  
    To eliminate click noises at positive or negative going transient.

11. **Add TP-8 (Q, 36-37)**
    
    For factory adjustment only.

12. **IC49, RAM 2101 and 5101**
    
    SN 202210-UP  
    Often, RAM 2101 is substituted by 5101 upon manufacturing or shipping replacement because of procurement problem.  
    RAMs of these models have different characteristics in timing response.  
    To make both RAMs compatible, factory modification on CPU board started with above Serial number. (See p.38 for detail.)

**NOTE:**

Besides suffix (A, B, etc.), the PCBs occasionally bear marks "A" and/or "B" above its code number to show the edition stands for 1, and a for 5, ex: example: a...  
8th edition.
GUIDES ON REPLACEMENT
MODULE CONTROLLER BOARD
(For early 500 units, see p.48)
When replacing OPH123 with OPH123A, be sure to proceed the following.
Check IC49 on both PCBs (being replaced and replacement) for name. If 2101 is on the existing PCB and 5101 on the replacement, take the modification illustrated below.
When replacing Upper board or Lower only:
Adjust VR1 [NOISE LEVEL] of unchanged MOD CON board to match the noise level of new board which omits the adjustment. Reconnect R21 of unchanged MOD CON, referring to drawing to the right. This will eliminate possible loudness differences between U and L voices.

IC49 OF MOD CON BOARD (MODIFICATION ON CPU BOARD)
(RAMs 2101 and 5101)
Below, two minor modifications (independent of RAM change) are also indicated:
Reconnection of IC37 and addition of 10UF at IC30 pin 8
Insertion of 5101 into a place previously occupied by 2101 requires pin 5 of IC23 on CPU board to be grounded. This reconnection as illustrated is to protect the data on panel control from garbled — while a control is being reset, some of other controls are also detected as moving; in extreme case no voice would sound. This is due to the fact that two RAMs differently respond to the same timing signal.
This modification has no adverse effect on 2101.
CIRCUIT DESCRIPTION
This circuit description applies to the JP-8 with serial numbers 171700 and up where DAC changed from 12- to 14-bit version, and concentrates on comptune program which is revised in line with the change.
This description makes reference to pages 6 and 7 "WIDTH" and "KCV" of the Circuit Description of First Edition issued separately.

WIDTH
P.6 Change title to WIDTH & TUNE
The coverage of the JP-8 keyboard is expandable to 96 keys using footswitch selector (RANGE SWITCH). In the following, KCV and key designation are defined as below.

In this mutual arrangement any KCV (VKn) at a key (Kn) is obtained from the equations:

\[ VKn = VKno + W \times (WIDSHTH) \times Kn \]

or

\[ VKn = T (TUNE) - W (84 - Kn) \]

where,

\[ W = 1/12 (V) \]

-- voltage steps per half tone

\[ T = VKn84 \]

In the following comptune, \( T \) is a reference voltage in calculating every KCVs to the equation (2) above.

Upon power on for the JP-8, comptune program starts frequency measurements at two points with MOD.A VCO-1 by applying KCV of Kn24(3V) and VKn84(8V) to it. If the VCO output is 20 cents higher than expected pitch at 3V KCV, and 30 cents lower at 8V as shown in the figure right, the factor \( W \) is given by:

\[ 8 - 3 (V) = (9570 - 3620) (cent) \]

Substituting 0.084 for \( W \) in equation (2) above would provide the VCO with KCVs for every keys, and the VCO will oscillate in 1V/oct steps with most of pitches slightly out of tune.
To bring each note in tune, the program first adds fine tune voltage (bias) ... \[ 0.084 \times 30 \]

\[ 100 \]

\[ = 0.0252 \]

\[ V  \]

To T. Then, finds KCVs for every notes by applying equation (2).

Example: VKn24 = 8.025(17) - 0.084(16) x (84 - 24) = 2.985V.

When compare this WIDTH with the WIDTH determined by previous 12-bit system, the new system provides more precise resultant because of wider measurement range.

INITIAL TUNING UPON POWER ON
When the power is first turned on for the JP-8, thermally unstable VCO tends to oscillate on frequencies which are greatly deviating from the expected frequency so that comptune circuitry will not be able to determine exact pitch error at a time. If a program encounters such a VCO, the program ceases measurement for that VCO but retains the data, then proceeds to the next VCO. After all the VCOs have been measured, the program resumes operation from the first VCO, depending on the previous data. However, the process is repeated only two times per oscillator, regardless of the frequency deviation. Properly functioning VCOs will be brought into tolerance at the second time. Most VCOs outside tolerances after completion of the second execution might be brought closer and closer to desired pitches if the comptune program is forced to repeat the operation by manual triggering of TUNE button. (See next paragraph.)

Tuning sequence is visually confirmed on flashing LEDs in the PATCH buttons.

However, when one PATCH LED stays on while MANUAL LED is flashing, they are indicating failure in that VCO. The comptune program cannot correct such a VCO as is indicated by a PATCH button as below, and does not proceed to the next VCO unless one of function switches is touched.

MODULE

VCO

<table>
<thead>
<tr>
<th>KEY</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
</tr>
</thead>
</table>

COMPUTE WITH TUNE BUTTON
When the comptune program is triggered manually with TUNE button (after power-on-tune), it runs only once for each VCO since the program already had data on fine tune, and drastic change in VCO frequencies is likely to occur. If the program fails to compensate frequency drift, iterative tapping of "TUNE" will bring VCO closer to correct pitch. Relying on this method is preferable only in an emergency; the cause of out of tune must be eliminated as early as possible.

KCV (INTERFACE BOARD)
P. 7 Lines 9 and 10: Delete
Lines 11-17: Reads as follows.
Each KCV data is represented in 14-bit format and is divided into two pieces -- MSB (most significant) 8-bit is latched by IC15 followed by LS 6-bit into IC13. DAC output has a range of 0-10V against 14 bits, thus resolution is 10V ÷ 2^14 (bit) = 0.66mV, nearly equals 0.7 cents in pitch. Durig I/V conversion in IC24, CV for EXT, jack is scaled 1V/oct.

CIRCUIT DESCRIPTION
P. 11: PUSH SWITCH SCANNING
Push switches (function switches with LED) are read every approximately 25ms (not 1ms). See timing chart on page 3 of the Circuit Description. LEDs are lit every 1ms when INT signal is applied from IC26 which in turn is timed by the signal generated at pin 17 of IC40. Failure of INT signal causes no LED driving signal, but has no relation to the switch reading performance.

<table>
<thead>
<tr>
<th>PATCH NO.</th>
<th>MODULE</th>
<th>VCO</th>
<th>MODULE</th>
<th>VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A</td>
<td>1</td>
<td>E</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>2</td>
<td>E</td>
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<tr>
<td>3</td>
<td>B</td>
<td>1</td>
<td>F</td>
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<tr>
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</tr>
<tr>
<td>8</td>
<td>D</td>
<td>2</td>
<td>H</td>
<td>2</td>
</tr>
</tbody>
</table>
CHANGES, MODIFICATIONS, ADDITIONS
INVOLVED IN IMPLEMENTING DCB
(Digital Communication Bus) BOARD
pp. 40-47

Top Panel
(072H078C)

KHC11026 (13189610)
SN272850-up

LED
LN5260A (15029409) SN242750-up independent of DCB installation

DCB BOARD
CPU BOARD

DCB BOARD
Panel F
Panel E
Panel C
Panel D
Panel A
Panel B
Panel G

BENDER PANEL
61-KEY KEYBOARD

Panel A

Holder (064H184)

DCB Connector
57-40140R (13429611)
Holder (064H153A)

Slide Switch
SSB 022-12RN (13159118)
Circuits Changes related to DCB Board Installation

CPU BOARD

Foil Side

Component Side

PANEL BOARD A

AX4
**Diagnostic Program in PROM D**

On the CPU board (of JP-8 furnished with the OC-8 or DCB board) located is IC33 (3.3D or 3.4D) which contains not only digital communication program, but also diagnostic program. The program, when executed in the TEST mode, simplifies testing and fault isolation of some of the ICs and their associated circuits listing to the right. For this program to run, the remaining PROMs (IC34–IC36) of CPU board must be of 3.2 version.

**PRECAUTIONS**

Allow plenty of time for warm-up (approx. 30 minutes).

If the CPU, PROMs or other circuits fail to perform their basic functions, the program will not start.

**STEPS**

1. Turn the JP-8 OFF.
2. To put the JP-8 into the TEST mode, either:
   a) Turn the power ON while pressing PATCH NUMBER buttons 1 and 3.
   or
   b) Set SI-1 and SI-2 of the Interface board to TEST, then turn the power ON.

The test program is executed in the order listed and is stopped whenever it encounters a defective IC (or a problem pertaining to a particular IC), and displays the suspected IC number in the window.

To resume the program, press any touch button. (For example, MANUAL.)

At the end of program, the window displays both the PROM D version and the DAC's bit format, for example:

- **33 12** -- 3.3D, 12-bit DAC
- **34 14** -- 3.4D, 14-bit DAC

**NOTES FOR TABLE**

1. 3.3D doesn't check IC5 and IC6.
2. Because of misprogramming, 3.3D will display these IC numbers in reverse order. If displayed, read IC20 as IC19, and IC19 as IC20.
3. Output from Module A VCO1-1 is applied to the DAC Check. Consequently, if this VCO fails, all the remaining tests will not be performed.
4. Push any button, and the version with D0 is displayed.
5. IC13 and IC15 on the 12-bit interface board are inversely numbered.
6. Read: IC13 as IC15, and IC15 as IC13.
7. If the 13-bit line malfunctions in the 14-bit D/A, the CPU concludes that the D/A is 12-bit, and skips the 13th and 14th bits.

**Description of Connection Cables**

In the below, SN refers to Serial Number of OP-8.

- For serial numbers up to and including SN220269, the OP-8 was provided with Flat Cable H146 for connecting the OP-8 to the JP-8.

- Effective from serial number SN220270, the OP-8 unit can be connected to the JP-8 through the Flat Cable H146 provided with the OC-8 unit, or to the JUNO-60 through the DCB Cable H165 provided with the OP-8 unit.

- Roland provides not only DCB Cable H165 but also DCB Cable H172 for interconnecting JP-8 or JUNO-60 as shown here.

- DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector. When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled. Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60. Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.

On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.
### PARTS LIST CHANGE

<table>
<thead>
<tr>
<th>PART. SERIAL NO.</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INTERFACE BOARD</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SN 171700 PCB Ass’y</td>
<td>OPH122</td>
<td>OPH122A</td>
<td>149H122A</td>
</tr>
<tr>
<td>Am6012 Latches</td>
<td>052H2B86</td>
<td>052H2B8</td>
<td>15219127</td>
</tr>
<tr>
<td>LSI755</td>
<td>LSI75</td>
<td>LSI75</td>
<td>15159512</td>
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<td>LSI755</td>
<td>TC4051</td>
<td>TC4051</td>
<td>1515913H0</td>
</tr>
<tr>
<td>IC25, IC26</td>
<td>LC02</td>
<td>TC4001</td>
<td>15159101T0</td>
</tr>
<tr>
<td>IC29, IC9 SN 212330</td>
<td>74LS74</td>
<td>4013BP (CMOS)</td>
<td>15159105T1</td>
</tr>
<tr>
<td>IC9</td>
<td>4013</td>
<td>TC4017H4P</td>
<td>15159610</td>
</tr>
<tr>
<td>ICs: ALL INCOMPATIBLE</td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>CPU BOARD</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SN 171700 IC34,IC36</td>
<td>µPD2716</td>
<td>µPD2716-JP8-A (IC36)</td>
<td>15179609 (version 3.x)</td>
</tr>
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<td>(version 1.0)</td>
<td>µPD2716-JP8-B (IC35)</td>
<td>15179610 (version 3.x)</td>
</tr>
<tr>
<td>SN 171700 IC34,IC36</td>
<td>µPD2716-JP8-B (IC35)</td>
<td>µPD2716-JP8-C (IC34)</td>
<td>15179610 (version 3.x)</td>
</tr>
</tbody>
</table>

| **MODULE CONTROLLER BOARD** |            |             |              |
| SN 202100 PCB Ass’y | OPH123     | OPH123A     | 149H123A     |
| OPH123A           | 052H2B69   | 052H2B6    | 15229802     |
| T1082             | 26A1015    | 26A1015     | 15119108     |
| Diocentreic       | 26C1815    | 26C1815     | 15119108     |
| Trs, 11, 12, 25  | R601611(RA1) | R601611(RA1) | 15119108    |
| TR26              | 2SA1015    | 2SA1015     | 15119108     |
| Switches          | 26A1015    | 26A1015     | 15119108     |
| SN 202210 IC49 RAM | 2101 only | 2101 or 6101 | 15179303     |
| (Compatible with minor modification, see pp. 37, 38.) |          |             |              |

| **PANEL BOARD F** |            |             |              |
| LED (display) SN 242750 | LN526RA | LN526OA | 15029409 |
| (Compatible but different in brightness and color; mix use should be avoided.) |          |             |              |

| **PANEL BOARD E** |            |             |              |
| SN 272860 Switches (LEDs) | KHC11091 (AR34235) | KHC11026 (SEL2210R) | 13169610 |
| (Switch proper remains unchanged. The new LED has better off-axis luminous density, mix use should be avoided.) |          |             |              |

### SN 282880-JP 8 WITH DCB BOARD

<table>
<thead>
<tr>
<th>PART NAME</th>
<th>FROM</th>
<th>TO</th>
<th>PART NO.</th>
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<tbody>
<tr>
<td><strong>TOP PANEL</strong></td>
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<td></td>
</tr>
<tr>
<td>Panel H78B</td>
<td>SN 171700</td>
<td>Panel H78C</td>
<td>072H078C</td>
</tr>
<tr>
<td>Chassis (jack)</td>
<td>SN 171700</td>
<td>Chassis H116A</td>
<td>06H116A</td>
</tr>
<tr>
<td>Holder (rear)</td>
<td>SN 171700</td>
<td>Holder H184</td>
<td>06H116A</td>
</tr>
<tr>
<td><strong>DCB BOARD</strong></td>
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</tr>
<tr>
<td>PCB Ass’y</td>
<td>OPH220</td>
<td>Holder H185</td>
<td>149H220 (pcb 052H380B)</td>
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<tr>
<td>Holder</td>
<td>74LS21</td>
<td>06H185</td>
<td>15169360</td>
</tr>
<tr>
<td>IC3</td>
<td>µPD2851AC</td>
<td>Flat Cable H12 (INTERFACE-CPU)</td>
<td>149H220 (pcb 052H380B)</td>
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<td>Flat Cable</td>
<td>Flat Cable H126</td>
<td>Flat Cable H213</td>
<td>053H213</td>
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<td>DCC Connector</td>
<td>SN 171700</td>
<td>Holder H153</td>
<td>1517911</td>
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<td>Holder</td>
<td>Sn 171700</td>
<td>Holder H153</td>
<td>1517911</td>
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<tr>
<td>Slide Switch</td>
<td>SN 171700</td>
<td>SSB-02-12RN</td>
<td>1517911</td>
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<tr>
<td><strong>CPU BOARD</strong></td>
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<tr>
<td>IC33</td>
<td>µPD2716-JP8-D</td>
<td>15179612 (version 3.4)</td>
<td>15179612 (version 3.4)</td>
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</tbody>
</table>

In order to expedite delivery of products or because of procurement problems, the factory is occasionally forced to make minor substitution of ICs. Such substitutions will work satisfactorily and compatible with the initial IC unless otherwise noted in related sections (circuit diagram, parts list, etc.).

**PART NUMBER**

Usually, equivalent semiconductors are assigned to the same part number as initial component with two-letter suffix identifying the manufacturer. For example, TO — Toshiba, ZO — Motorola. In ordering such ICs, uncertain suffix can be omitted from the part number, and the factory will supply suitable ones with notes or cautions, as necessary.

Parts on the EQUIVALENT

<table>
<thead>
<tr>
<th>PARTS LIST</th>
<th>Equivalent</th>
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<tr>
<td>TC4052BP</td>
<td>HD14052BP</td>
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<td>TC4051BP</td>
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<td>TC40175BP</td>
<td>µPD41758C</td>
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<tr>
<td>µPD2101ALC</td>
<td>MSL2101ALC</td>
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<tr>
<td>µPD5011LC</td>
<td>MSL5011LP-1</td>
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<tr>
<td>µPD780C-1</td>
<td>LH0080A</td>
</tr>
<tr>
<td>µPD2716D</td>
<td>MSL2716K</td>
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<tr>
<td>µPD444C</td>
<td>MSL9881P-45</td>
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<td>µPD2114C</td>
<td>MSL2114LP</td>
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<td>µPD8253C</td>
<td>MSL8253P-5</td>
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<td>TL082CP</td>
<td>NJM082CP</td>
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<td>µPC4082C</td>
<td>MSL2114LP</td>
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<td>(exp. 7406)</td>
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APPENDIX

PCB EDITION

Dot and circle above PCB code are indicative of edition; "●" stands for 1, and "○" for 5. Example: ● = 6th edition.

Illustrated on pp. 48-50 is information on MODULE and MODULE CONTROLLER Boards mounted on the JP-8 models with serial numbers up to 090599. For circuit diagram, refer to p.11 or p.12 although some small discrepancies may exist.

CAUTION ON REPLACEMENT OF PCBs IN THIS SECTION

Although terminal for terminal compatible, when mixed use, new and old PCBs process signals in slightly different way, reproducing voices that are distinguishable form each other. Therefore, when replacing MODULE or MOD CON board in this section, use a set of PCBs of the same edition group as described below.

NOTE: Replacement of MODULE board can be made independently of MOD CON board, and vice versa.

MODULE CONTROLLER BOARD

<table>
<thead>
<tr>
<th>Group</th>
<th>PCB Code</th>
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<tbody>
<tr>
<td>A</td>
<td>052H269 or 052H269</td>
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<tr>
<td>B</td>
<td>052H269-up 052H270-up</td>
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</tbody>
</table>

MODULE BOARD

When replacements for MOD CON are of group B, check 1C49 (RAM) for name. If it is 5101, see p.38 for necessary modification.

Listing below are descriptions of surface mounting, jumper wire, and conductive foil cut made on the MOD COM boards up to the abovementioned serial numbers, shown on the next page.

ABBREVIATIONS

C-pattern cut  Diode  R-resistor  J-jumper  M-mylar cap

Serial numbers

1B-050199  2A-050200  2B-060209  3A-060300  4A-070400  5A-080500  5B-090599

<table>
<thead>
<tr>
<th>No.</th>
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<th>No.</th>
<th>Part</th>
<th>SN</th>
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<tr>
<td>1</td>
<td>C</td>
<td>up to 26</td>
<td>10</td>
<td>R</td>
<td>5A-up</td>
</tr>
<tr>
<td>2</td>
<td>C</td>
<td>3A-5B</td>
<td>11</td>
<td>R</td>
<td>3A-5B</td>
</tr>
<tr>
<td>3</td>
<td>C</td>
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<td>12</td>
<td>D</td>
<td>2xC</td>
</tr>
<tr>
<td>4</td>
<td>D</td>
<td>up to 1B</td>
<td>13</td>
<td>R</td>
<td>3A-5B</td>
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<td>5</td>
<td>R</td>
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<td>14</td>
<td>J</td>
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<tr>
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<td>J</td>
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<td>15</td>
<td>M</td>
<td>4A-5B</td>
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<td>7</td>
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<td>J</td>
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<td>17</td>
<td>M</td>
<td>3A-5B</td>
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<tr>
<td>9</td>
<td>R</td>
<td>up to 2B</td>
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</table>
MODULE BOARD OPH124
SN 030100-090599 (pcb 052H270 or 052H270)