**JUNO-60 SERVICE NOTES**

**First Edition**

### Specifications

- **Keyboard**: 61 keys, 5 octaves
- **VCF**:
  - RESONANCE (0 - Self Oscillation)
  - KEY Follow (0 - 100%)
- **ENV**:
  - ATTACK Time (1ms - 3s)
  - DECAY Time (2ms - 12s)
  - SUSTAIN Level (0 - 100%)
  - RELEASE Time (2ms - 12s)
- **LFO**:
  - RATE 0.3 - 20Hz
  - DELAY TIME 0 - 1.5s
- **ARPEGGIO**:
  - RATE 1.5 - 50Hz
  - MEMORY PATCH NUMBER (1 - 8)
  - BANK (1 - 7)

### Rear Panel

- **Output Level**
  - (L): -30dBm/M: -16dBm/H: 0dBm
  - ARPEGGIO CLOCK Input
    - (1 step/pulse +2.5V or more)
  - TUNE (50 Cents)
- **Dimensions**
  - 1060 x 378 x 113mm
  - W x D x H
  - 41-3/4 x 14-7/8 x 4-7/16in.
- **Weight**
  - 12kg/26lbs. 7oz.
- **Power Consumption** 30W

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### Parts Location (Top)

- **Pot. EVH-OTA515B14**
- **Jack (Stereo)** HJ3231-01-20 (13449224)
- **Switch** ISW-0372-01-520 (13159332)
- **Holder** (064A184) Black or (064A164) Nickel
- **Connector** 57-40140-R (13429611)
- **Top panel** (072H132C)

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### Parts Location (Inner)

- **JACK BOARD**
  - OPH190 (149H190)
- **Power transformer**
  - 02B057 (100V/117V/220V/240V)
- **Power switch**
  - 1801-0121 (14149102) or WKA44 (13149108)
- **CPU BOARD**
  - OPH161 (149H161)
  - OL124 (15020103)
  - PG1 (08H264A)
  - Side panel (08H052)
  - CPU BOARD 0PH161 (149H161)
  - Panel board A 0PH187 (149H187)
  - Panel board B 0PH188 (149H188)
  - Cabinet (08H264A)
  - Rubber foot G-5
  - Holder (064A154B)
  - Power supply board PSH084 (100V/117V)
  - PSH084 (220V/240V)
  - PSH085 (220V/240V)

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CHANGE INFORMATION (Panel Board B)

See circuit diagram for details.

1. Pattern Re-layout (SRU53R00 up)
   Provide foil pattern exclusive to display signal return (terminals 81/31) on 052H411C. This additional pattern substantially relieves audio signal from noise.

2. IC6 Reconnection (SRU65500 up)
   Pull up pin 2 of IC6 to guard pot data from digital noise.

3. IC2 Reconnection (SRU65500 up)
   Decrease LPV amplitude to eliminate overmodulation.

4. Change RAM IC11 and IC12
   (SN undefined)
   From TC5516AP to TC5515AP-20 or µP044AC-1 for positive memory storage.
NOTES: UNLESS OTHERWISE SPECIFIED
1/2 TA75558S
1) ALL NPN TRANSISTORS ARE 2SC1815 (GR or Y) or 2SC603 (F)
2) ALL PNP TRANSISTORS ARE 2SA1015 (GR or Y) or 2SA1115 (F)
3) ALL FET TRANSISTORS ARE 2SK30A (GR or Y)
4) ALL DIODES ARE 1S2473
CIRCUIT DESCRIPTIONS

CPU BOARD

KEYBOARD AND SWITCH (NON PROGRAMMABLE) SCANNING

The CPU IC58 on the CPU Board applies sequential scanning data (in the leftmost column in Table 1 below) to Address Decoder IC58, setting its appropriate output pin low. Each pin will be connected to port 1 through switch contacts being closed and through inverters IC53 and IC57. The combination of highs and lows at port 1 pins tells the CPU which key is pressed, not pressed, or which position the switches are set.

Note: TRANSPOSE switch on Bender Board is not read directly but through SW LATCH IC9 on Panel Board B. TRANSPOSE is scanned beforehand together with the programmable switches by another CPU on Panel Board B.

The CPU IC56 stores two kinds of program for use in different applications, and knows its application at the very first of the scanning cycle. After power reset, the CPU first issues bits 1001 (see top of Table 1) and knows that voices to be assigned to keys played are 6 (L, H, L at Port P10-P12) and that the model it is now installed is the JUNO-60 (L at P17). If the CPU malfunctions, voltages on these port pins and associated circuits (including D20) should be checked.

```
BUS 6563 0 1 2 3 4 5 6 7
0000 C C D D E F F F G
0001 G A A A C C D D
0010 E F F F G G A A B
0011 C C D D E F F F G
0100 G A A D D B C C D D
0101 E F F F G G A A B
0110 C C D D E F F F G
0111 G A A B C I(D) I(D) I(D)
1000 TRANSPOSE ARR & KEY ASN.
1001 L H L not in use L
```

Table 1

KEY ASSIGNMENT

Six channels are assigned to the keys played in the order CH1-CH6, in the cyclic manner, that is, when the 7th key is played while previously played 6 keys are still held, the 7th key steals the first voice.

Three more assignment modes are provided for test purpose. See Adjustment section of this manual.

DIGITAL COMMUNICATION

The JUNO-60 is furnished with a DCB interface for linking with external digital instruments. When the DCB interface circuit on Panel Board B is engaged in communication, it coordinates the transfer of data between two instruments by applying Low to INT of the CPU on the CPU Board (will be detailed under DCB Interface section).

SOUND SOURCE

When a key is played on the keyboard, the CPU (CPU BOARD) provides a set of independent data — Divider for the programmable counters (IC54, IC56) and CV for WAVEFORM and VCF, to keep the voices sound alike with pitch differences corresponding to a key held. Fig. 1 shows a simplified block diagram of sound source system, for clarity.

```
Fig. 1
```

Master Oscillators TR58-TR62

An LC oscillator having a variable capacitance diode (D18) to which control voltages from BENDER, LFO and TUNE, — common to all the VCOs, are supplied.

Variable range:
BENDER -0.700 cents
LFO -1.300 cents
TUNE -0.500 cents

When these voltages are summed together, the maximum shiftable range of the master oscillator is ±1050 cents or from 1MHz to 3.5MHz with the center frequency at approximately 1.9MHz. The output signal is routed to programmable counters IC54 and IC56 through TR63.

Programmable Counters IC54 and IC56

Programmable counter 8253 containing 16-bit counters is capable of dividing high frequency signals, generated at the Master oscillator, by up to 65536. Assume that the master oscillator runs at 1902810Hz and a divisor is 4306, the counter develops 442Hz rectangular signals. Each time key(s) is played, the CPU extracts division data for that key from the internal PROM and delivers it to DATA IN of the counters in 8 bit x 2 format.

Waveform Conversion

SAWTOOTH GENERATOR

Analog voltages (a series of 6 key control voltages for 6 channels) from D/A converter will change in 0.48oct steps as different keys are played. KCVs are combined with voltages from TUNE, and LFO and BENDER if any, and are fed to anti-log amplifier TR56. The summed voltage increases or decreases in 1V/oct steps at TR56 output, which is passed on to one of S/Hs (IC33-IC35) selected by analog Demultiplexer IC36. C7 charges (current) in proportion to CV coming on inverting input pin of IC16 and discharges through TR5 through the rate of square wave generated from programmable counter (IC54 or IC55), maintaining the sawtooth amplitude constant over the frequency range.

VARIABLE PULSE WIDTH

Besides its direct application as sound source, sawtooth generator also serves as a source for asymmetrical square wave. Sawtooth wave is routed to (-) pin of comparator/S&H circuit where the voltage on (+) pin determines the sampling period of the sawtooth wave thus duty cycle of the square wave.

```
Fig. 2
```

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SUB OSCILLATOR

Square wave from programmable counter is also delivered to flip-flop where it is divided in half, and applied to TR4 base. The amplitude of TR4 output can continuously be varied by setting of SUB VR20 on Panel Board A.

VCF Control Voltages

While 6 contour voltages developed at ENV generator are running directly to mated VCA's on the exclusive line, they are multiplexed and carried through a common bus together with other control signals for VCF application. On the input pin of summing amp there is another multiplexed voltage (KCV) from D/A converters IC51-IC53 on CPU Board. These multiplexings are synchronized for stable data travel.

PANEL BOARD B

CPU µPD80C49C-028

<table>
<thead>
<tr>
<th>DESIGNATION</th>
<th>PIN NO.</th>
<th>FUNCTION</th>
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<tr>
<td>DB 12  Data Bus</td>
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<td>Prog SW Scan/Display Drive</td>
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<tr>
<td>13</td>
<td>RAM Address</td>
<td></td>
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<tr>
<td>14</td>
<td>RAM Data</td>
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<td>15</td>
<td>Slider and Switch Data</td>
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</tr>
<tr>
<td>16</td>
<td>A/D Data</td>
<td></td>
</tr>
</tbody>
</table>

PORT 1 P18 26,27

| PORT 2 P26 | 21 | 4051 x 4 Address (MPS, INP) |
| 22 | RAN x 2 Address |
| 23 | Chip Select |
| 24 | 4051 CS x 4 |
| 25 | 4017A, TC40287F VR Enable |
| 26 | 4017A, 408273 Latch Pulse |
| 30 | Tape Interface Output |

Table 2

The flowchart (Fig. 5) will be an aid in reading the description in this section.

1. When a new BANK/PATCH button is pressed, the CPU calls "Read RAM" subroutine.
   When BANK, PATCH and WRITE buttons are pressed, the CPU calls "Write RAM" routine.
2. When the CPU finds a certain amount of discrepancy between the preceding reading and the new reading, it sets Edit Flag and updates the data being delivered.

SWITCH READING

The matrices for the programmable switches and memory switches are located on Panel Boards A, B and Bender Board. They are busied together on Panel Board B. The bus is divided into five sections with maximum eight switches per section. Each bus section and switch contact are connected to the CPU on Panel Board B: bus section through Latch IC15 (latched on PROG) and through Decoder IC16, contact through Port 1. The CPU maintains a serial data output (from DB) and reads the results from Port 1, in the same manner as described previously under KEY SCANNING.
**SWITCH DATA OUTPUT**

Of the switches read during the above switch scanning, 11 programmable switches are organized in 14 bit group in the CPU and are divided into two fields when being sent out from the CPU. At the very end portion of the program loop, the CPU first issues 6-bit data on the data bus and IC13 latches it into IC8 with ALE. Then the next 8 bit is directly fed to IC9. IC8 and IC9 latch out 14 bit data at the same time when the Port 2 presents bits X1110XX.

It should be noted that TRANSPOSE information only is routed to and involved in the CPU Board switch matrix for further processing, while the remaining switch data are delivered directly to respective destinations.

**POTENTIOMETER MULTIPLEXERS AND ADC (PANEL BOARDS A, B)**

**MULTIPLEXER**

All 16 programmable pots are divided between Panel Boards A and B, with each 8 pot group connected to an associated Pot Multiplexer, Pot MPX and ADC (Analog to Digital Converter) allow the computer on the Panel Board B to read and therefore to store the knob settings into RAM for a patch. Addresses specifying the pots to be sampled are fed from Port 2 as shown in Fig. 7. Pot MPX program starts with VR17 DELAY TIME when INH is applied from Latch IC19 on Panel Board B. The MPXIC IC27 (Board A) sequentially connects each pot wiper (on Board A) to the ADC which represents analog equivalent of Pot Value in 8-bit format.

**ADC**

The ADC is based on a Successive Approximation consisting of DAC, comparator and CPU’s internal “register”. To convert a Pot value the CPU (Board B) first issues 100000000 on the data bus. IC13 latches MSB which is weighted by ladder resistors, converted to 2.4V of analog equivalent then passed on to non-inverting input pin of IC6, comparator. Being fed lower voltage on (+) input than on (−) input signal being compared, the comparator turns its output low, telling the computer to keep MSB high. Then the CPU places the next bits 11000000 which causes (−) input of the comparator to rise to 3.6V, which, in turn caused comparator output to turn high, resetting DB6 to 0.

In the same manner the CPU compares all the bits down to DB0 against the comparator’s (−) input signal and establishes the digital data for that Pot value.

This procedure is repeated 16 times for all 16 pots.
### POT DATA OUTPUT

An 8-bit data representing pot setting is placed on the CPU bus 16 times for each pot. Each 8-bit is latched by IC13, D/A converted by R2R and sent to IC3 and IC8 (POT DIMPLXER) on Board A, where it is distributed to a channel addressed by port 2.0.2.3 of the CPU (Board B) at a sampling rate of INH from IC15 (Board B).

![Diagram of POT DATA OUTPUT](image)

### DISPLAY LED LIGHTING

Being an I/O port, the Port 1 changes its state to output mode immediately after finishing switch readings, delivering display LED driving signals to LED board. Alternately swinging outputs pins 9 and 10 of IC16 allow upper and lower LEDs to conduct at duty cycle of nearly 50 of dynamic lighting. The period 7.2ms in the timing chart (Fig. 10) is the time required for the CPU to complete one program loop.

![Diagram of DISPLAY LED LIGHTING](image)

### MEMORY

Two identical RAMs (4K bit – 4x1024) make up the patch memory, which can store up to 1K byte (8x1024 words). Each memory cell is addressable with 10 bits. MSB 2 bits come from ports 2.0 and 2.1. The remaining LSB 8 bits from Data bus are latched into RAMs by IC13 with ALE. RAM chip select (CS) is accomplished under the conditions Port 2 = X1111XXX

- WR or RD = low
- RESET = high

The CPU can extract RAM memory only when WR is ANDed with PROTECT at IC18.

![Diagram of MEMORY](image)

### TAPE INTERFACE

The CPU (Board B) transfers the programmed data to or from a cassette recorder through Interface circuitry at approx. 340 baud (340 bits/s).

![Diagram of TAPE INTERFACE](image)

### SAVE

Pressing SAVE button allows the CPU to convert a set of patch data to square waves: 0 (space) to four cycles of 1.38kHz and 1 (mark) to seven cycles of 2.38kHz, and to send them from Port 2.7. The modulated bits are applied through IC21E (inverter) to IC22A (LPF) where their high order harmonics are rolled off by 12dB/oct slope and lower components by C22 (6dB/oct HPF) before being passed on to SAVE jack.

![Diagram of SAVE](image)

### DCB (Digital Communication Bus)

The JUNO-60 can be controlled from the external equipment which transmits the control voltage in the form specified in this section. The JUNO-60 can also control an external "musical instrument" which accepts data made in the form described in this section. The CPU on the CPU Board communicates with an external equipment through DCB (Digital Communication Bus). IC24 on the Panel Board B interfaces them (CPU and EXT instrument).

### INTERFACE

The IC24 is the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. In the JUNO-60 the 8251A is configured as Asynchronous Receiver/Transmitter (USART). The 8251A will signal the CPU (on the CPU Board) whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of 8251A, when INT goes low under one of the following conditions, by turning C/D to high (1) and READ to low (0), entering Interrupt Handling Routine.

**INT LOW CONDITIONS:**
- RxRDY = 1 (H)
- or RxEMPTY = 1 (H) and TX BUSY = 1 (H) (DCB connector)

* RxRDY: 1 (H)

This output indicates that 8251A contains a character that is ready to be input to the CPU, requiring the CPU to accept the data.
**DCB DATA FORMAT**

The Data format described in this section is commonly applicable to Roland products furnished with the DCB connector. Variations unique to individual models and problems which might happen in linking the JUNO-60 to other DCB instruments will be discussed in more detail later.

**GENERAL SPECIFICATIONS**

* BLOCK

Basically, a block is comprised of three codes: One Identifier, one or more Data Codes and one End Mark. The transmitter can send a block (containing identical information) either continuously or intermittently at 10ms–100ms intervals to assure stable information transmission. In an intermittent transmission system, the transmitter must send a new block upon occurring of change in the information. The new block must contain both changed and unchanged data.

* IDENTIFIER

At the head of each block is a 1-byte identifier which uses a value within $0F1H$ (241) through $0FEH$ (254) to signify the kind of DATA CODE that follows, $0FDH$ (253) -- PATCH CODE, $0FEH$ (254) -- KEY CODE, others are undefined. Any data which follows an Identifier must not include these values.

* DATA CODE

A Data code is comprised of a section or series of sections (each 1 byte, called channel–04) containing the information defined by the identifier. The code length (number of channels) depends on circuit configuration of the transmitter. Once a communication is established over DCB, the code length and the transmission order of the channels should not be changed throughout the communication.

Some identifiers will be accompanied by the code of predetermined length. (Exp. PATCH CODE--1 byte.)

* END MARK

An End Mark is necessary unless the code length is predetermined by the identifier or the block is to be automatically terminated by the identifier of the next block.

* DATA PROCESS

The receiver begins processing data code at the moment it accepts the End Mark or the Identifier at the head of the next block.

**DETAILED SPECIFICATIONS**

This part mainly discusses the Key Code, only which the JUNO-60 deals with and problems that may arise in linking the JUNO-60 to other DCB instruments, etc. OP-8 and JP-8. Some differences in the data format and transmission will exist between models.

* BLOCK

The JUNO-60 transmits blocks continuously, while the JP-8 and OP-8 intermittently.

* IDENTIFIER

Two Identifiers are already defined:

- **0FDH (253):** Patch Code
  
  Indicates that the code is 1-byte format representing Patch Number or Patch Preset Number.
  
  This code is employed in the JP-8 and the OP-8. The JUNO-60 does not deal with this code. It ignores the data following this identifier.

- **0FEH (254):** Key Code
  
  This signals the receiver that the following data is for key information (key number and gate).
  
  The length of the data:
  
  - JP-8 and OP-8 = 8 bytes
  
  - JUNO-60 = 6 bytes

* DATA CODE

Patch Code

The JP-8 and OP-8 send this code together with the Key Code for each change in Patch data and do not transmit it again. This block does not accompany End Mark.
Key Code

The Key Code is preceded by the Key Code Identifier (OFEO 254). Since the JUNO-60 is so configured that it accommodates only Key Code, the CPU (CPU BRTD) returns to the main routine if identifier bits is other than OFEO, ignoring the subsequent data.

The transmitter assigns the keys played on its keyboard to individual channels, coding each key information in 8-bit format where MSB 1 bit represents GATE ON (1) or OFF (0). The remainder (7 bits) represents key designation (name) listed in the table below (Fig.17) (Hexa-decimal). Then, the transmitter places all the channels on the DCC sequentially in the order of its key assign mode. The receiver, upon receiving channels, assigns its voices to them by its own key assign mode which will differ between models. Fig.17 shows some rather distinguishable key assignments. The transmitter need not delete the unnecessary channel(s), instead it turns MSB to 0 (GATE OFF).

![KEY ASSIGN TO BUILT-IN & EXTERNAL KEYBOARDS](image)

When "external keyboard" is connected to the JUNO-60 through the DCC, the CPU recognizes it as one being connected to the built-in keyboard in parallel and assigns its voices to whichever the key played on both keyboards. However, if two keys of the same note are played at a time on both keyboards, the program gives priority to the key first played as long as the GATE is ON. This fact may trick the player when he plays the JUNO-60 with SUSTAIN set shorter than the gate duration of the note being reproduced. For example, if he plays C4 right after the C4 note activated by DCC dies away, it doesn’t sound. To retigger the gate both keys must once be made OFF, then one key is pressed again.

KEY CODE INCLUDING MORE THAN SIX CHANNELS

What will happen if more than 6 channels are fed from the external keyboard to the JUNO-60? In this case, 7th and subsequent keys have to wait until reserved channels are cleared, either by releasing of keys or by software. The software steals a voice from a channel whose gate first turned ON among 6 channels. Then the program assigns the voice again to 7th channel and so on as new channels are coming. This feature enables the JUNO-60 to accept limitless channels within a key code. Contrast to this, the JP-8 can receive 8 channels only at a time.

LINKING DCB DEVICES

Two cables are available for connecting DCB units, DCB Cable H172 and H165.

DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector. When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled. Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60. Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.

On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.

GROUND LOOP NOISE

Because of the AC ground, a "ground loop" may be created when the DCC cable is connected between the JUNO-60 and its party (equipment). As a result, a certain-level digital noise may occur. In the later JUNO-60 the noise is considerably reduced by rearrangement of ground paths together with installation of Panel Board B of improved version, 052H411C (pattern relayout).

The modification is conducted at the factory on the units with serial numbers 263000 and subsequent. For the units prior to SN263000, alternative modification can be made for the purpose of noise reduction. See Fig.19.

Note: This modification has no effects on the later units.

Caution: Do not disconnect GND from DCB connector (Pin 4). Floating digital GND path may induce noise in other signal path.
RAM MEMORY TEST

The JUNO-60 has RAM TEST Program. In the RAM test mode, the program writes to each RAM chip and reads the data back to find any defective memory cell that may exist in the RAMs. If there is an error, the memory address will be displayed in the PATCH NUMBER window in Hexadecimal figure, as example below. (Fig. 21)

Caution: * All programmable data will be erased during the test. Save them on tape before testing.
* RAM should not always be defective if indicated by “error display”. Check DATA BUS and their associated ICs, Trs, etc. for short or open.

HOW TO RUN TEST PROGRAM

1. Set controls as indicated by arrow.
2. Insert a bare plug into PATCH SHIFT jack on the rear panel to open the circuit.
3. While pressing CHORUS OFF and II buttons, switch the power on.

The program starts with the lowest address, so if a RAM is seriously defective, it displays “00” and stops there. When program sees an error, it won’t stop to the next address unless correction is made.

Fig. 20

If no defect is found in the RAM during the test, write data B1 (a continuous square wave sound) into all of the tone numbers so that Manual symbol $E.3$ will be displayed in the LED Display.

RAM ADDRESS INDICATION (000-3FF) LOWER BITS (00-FF)

EXAMPLE

000-0FF (Example $01F$)
000-1FF (Example $13E$)
200-2FF
300-3FF  Fig. 21

M54528P
7-Segment Driver

TC40H393P
Dual 4-bit Binary Counter

Circuit Diagram

TA7555S
TA75559S
OP-Amp

<table>
<thead>
<tr>
<th>COUNT</th>
<th>QA</th>
<th>QB</th>
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<th>QD</th>
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20
TEST PROGRAM

For easier adjustment, the two CPUs in the JUNO-60 store the Test Programs. The JUNO-60 ADJUSTMENT PROCEDURES basically use these Test Programs. However, if no Test Mode (or Patch Number) is specified for a particular adjustment, the adjustment is to be performed manually.

TEST MODES

1. Key Assign (CPU BOARD)

To enter the Test Mode, hold the KEY TRANSPOSE button down, turn the POWER ON, and then continue holding the KEY TRANSPOSE button down for 2 seconds. The 3 Key Assign Modes can be selected through the ARPEGGIO MODE selector.

UP (UNISON): Six voices are assigned to the same key simultaneously.

UP & DOWN (ROTARY): The CPU assigns channels (voices) in a cyclic order (i.e., 1, 2, 3, 4, 5, etc.) to the keys (or repeatedly-struck single key) being played (legato or staccato) and remembers the last channel even after the key is released. New assignment will start with the next channel. Note that the first key does not always activate CH1.

DOWN (NON-ROTARY): If a second key is pressed while one key is pressed, CH2 is activated. If any preceding keys are open, the channel with the smallest number takes priority for the next assignment. For example, if any 4 keys are pressed, (activating CH1-CH4), then 3 keys released (including the first key), and one key again pressed, CH1 will again be activated.

To escape the Test Mode, turn the POWER OFF and wait 3 seconds before turning the POWER ON again.

Note: There are 2 adjustment methods: (1) using test point T4M, etc., and (2) listening to a sound(s) through the OUTPUT jack. Also, CH2-CH4 can be adjusted by listening to the best sound between channels. Perform these audible adjustments in the NON-ROTARY Key Assign Mode by setting ARPEGGIO to DOWN. For example, in order to produce sounds at CH1-CH4, sequentially hold keys 1 through 4, and release keys 2 and 3. (Fig. 23) If HOLD button remains ON, an extraneous sound will be heard. Turn HOLD button OFF as necessary.

2. Patch Number (PATCH BOARD B)

Insert a bare plug into the PATCH SWITCH jack in order to open the Jack Circuit. The CPU on the Panel Board B then enters the Test Mode, displaying a meaningless “111” in the Patch Number Display window. As a result, the Panel Setting Programs used for the adjustments, which are stored in BANKS B and C, can be read. To call BANK B, hold BANK button 5 down and press 3.

Note: The Patch Number does not have to be set unless otherwise specified.

Edit Mode

In the Test Mode, once a Patch Number is selected, the visual panel setting has no relation to the sound being reproduced. However, some panel controls may need resetting for editing purposes, since the same Patch Number may be used as the basic setting for several adjustments. For example, when a control is to be set to “1” and the control is already in position “1”, it may actually be set to “3” by the CPU. In this case, move the control until the 2 dots in the Patch Number Display window light up, then return the control to “1”.

Caution: Before performing adjustment, check to see if the Edit Mark is displayed in the Patch Number Display window. If the Edit Mark is displayed, select any other number, then again select the desired Patch Number.

Table 5

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<th>N</th>
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Fig. 22 Key Designation

Table 6 Panel Control Settings by Test Program
ADJUSTMENT PROCEDURES

1. POWER SUPPLY VOLTAGE
   (POWER SUPPLY BOARD)

   Use a digital voltmeter with a resolution of millivolt.
   (1) Adjust VR1 for +15V ± 10mV at “a”.
   (2) Check the voltage at “b”. It should be -14.5V to
   -15.5V.
   (3) Check the voltage at “c”. It should be +4.5V to
   +5.5V. Refer to Fig. 24.

2. MASTER OSCILLATOR (CPU BOARD)

2-1. BIAS

   Test Point: TP2
   (1) Connect digital voltmeter to TP2.
   (2) Adjust VR39 for +7.1V.

2-2. TUNE

   Test Point: OUTPUT
   Patch Number: 82
   Test Mode: UP
   Control: TUNE (REAR PANEL) = center
   (1) Connect Tuner, strobe, or other suitable equipment to OUTPUT jack.
   (2) Hold down A4 key and adjust L1 for 442Hz using a nonferrous tool.

3. BENDER (BENDER BOARD)

   Test Point: OUTPUT
   Patch Number: 82

   Note: Check to see if Edit Mark is ON. If so, select
   another Patch Number and again select “B2” (see “Patch Number” section).

   Test Mode: UP
   Control: DCO (BENDER PANEL) = 10
   (1) Connect proper tuning system to OUTPUT.
   (2) Press HOLD.
   (3) Press E5 key. Hold BENDER lever in leftmost position and adjust – ADJ VR1 for 442Hz.
   (4) Press HOLD again. Press D4 key.
   (5) With BENDER lever in rightmost position, adjust +ADJ VR2 for 442Hz.

4. SAWTOOTH (CPU BOARD)

   Test Point: CH1 TP3 (Rightmost TP3 on CPU BOARD)
   Patch Number: 82
   Test Mode: UP
   Controls: HOLD = ON
   OCTAVE TRANPOSE = DOWN

   Note: If OCTAVE TRANPOSE is already in DOWN, reset it to NORMAL or UP, then
   to DOWN. This is for editing (see “Edit Mode” section).
   (1) Press C2 key and adjust VR38 for 12Vp-p.
   (2) Press G7 key and adjust VR37 for 12Vp-p.
   (3) Press other key(s), and confirm 12V ± 1Vp-p.

   Note: Reset OCTAVE TRANPOSE to NORMAL for the remaining adjustments.

   Caution: This adjustment will affect item 9, the PWM ADJUSTMENTS.

5. VCA (CPU BOARD)

5-1. GAIN

   Test Point: TP4 pins 1–6 (CH1–CH6)
   Patch Number: 82
   Test Mode: UP
   Control: HOLD = ON
   (1) Connect oscilloscope to TP4 pin 1 (CH1).
   (2) Press C4 key and adjust VCA GAIN VR4 of
   CH1 for 4Vp-p.
   (3) Repeat steps (1) and (2) for TP4 pins 2–6
   (CH2–CH6).

5-2. OFFSET

   Test Point: TP4 pins 1–6 (CH1–CH6)
   Patch Number: 83
   Test Mode: UP

   HOLD = ON
   ARPEGGIO = ON

   Table 25

   (1) Connect oscilloscope (with V gain at maximum)
       to TP4 pin 1 (CH1).
   (2) While pressing any two keys, adjust OFFSET
       VR5 of CH1 so that the pulses are minimized.
       (Fig. 20)
   (3) Repeat steps (1) and (2) for TP4 pins 2–6
       (CH2–CH6).

   Caution: While adjusting PANEL BOARD A, use a
   screwdriver with a short shank to avoid short-circuiting to the heat sink of
   the POWER SUPPLY BOARD.

   Test Point: TP4 (CPU BOARD)
   Patch Number: 82
   Controls: NOISE = 10
   HIGH (PWM) = OFF

   While pressing any key, adjust NOISE LEVEL VR14
   (PANEL BOARD A) for 4Vp-p. (Fig. 27)

6. NOISE (CPU BOARD/PANEL BOARD A)

   Caution: While adjusting PANEL BOARD A, use a
   screwdriver with a short shank to avoid short-circuiting to the heat sink of
   the POWER SUPPLY BOARD.

   Test Point: TP4 (CPU BOARD)
   Patch Number: 82
   Controls: NOISE = 10
   HIGH (PWM) = OFF

   While pressing any key, adjust NOISE LEVEL VR14
   (PANEL BOARD A) for 4Vp-p. (Fig. 27)

7. LFO (PANEL BOARD A)

   Preset the following controls for LFO adjustments
   unless otherwise specified.

   Table 28

   Test Point: TP19 (PANEL BOARD A), Terminal 36
   (PANEL BOARD A) or Terminal 20
   (BENDER BOARD)

   7-1. RATE

   (1) Set oscilloscope to 10ms/cm, 2V/cm.
   (2) Adjust LFO RATE VR1 for 45ms. (Fig. 29)

   7-2. GAIN

   (1) Set oscilloscope to 10ms/cm, 2V/cm.
   (2) Adjust DCO LFO GAIN VR2 for 14Vp-p.
       (Fig. 20)

   7-3. OFFSET

   (1) Set oscilloscope V gain at maximum.
   (2) Set TRIG MODE to MAN (Manual).
   (3) Adjust DCO LFO OFFSET VR3 so that the
       horizontal line rests on the GND potential.
       (Fig. 30)
7.4. DELAY

Note: HOLD must be OFF.

(1) Reset TRIG MODE to AUTO. Set DELAY TIME to "00".
(2) Set oscilloscope to 2V/cm, 0.5s/cm.
(3) Adjust DELAY TIME VR4 so that when a key is pressed, the waveform disappears; then 2 seconds later, begins to reappear. (Fig. 31)

8. VCF (CPU BOARD/PANEL BOARD A)

Note: VCA adjustments must have been completed.

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

8-1. RESONANCE

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: B4
Test Mode: UP

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press any key and adjust RES VR1 (CPU BOARD) for 4Vp-p. (Fig. 32)
(3) Repeat steps (1) and (2) for TP4 pins 2–6 (CH2–CH6).

8-2. FREQUENCY

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: B4
Test Mode: UP

Note: FREQ VR2 of CH1 (CPU BOARD) should not be set too close to FCW or FCOW position.

8-3. KYBD OFFSET

Patch Number: B4
Test Mode: UP

Note: Either method (I) or (II) can be used as desired.

(I) Test Point: TP4

Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
Press C4 key.
Set KYBD to "10" and adjust KYBD OFFSET VR1 (PANEL BOARD A) for 24Vp-p.

(II) Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)

Control: HOLD = ON

Press C4 key.
While repeatedly moving KYBD to "10" and "0", adjust VR11 (PANEL BOARD A) so that the voltage variation is mini-

Note: This adjustment can be made by listening to the sound from the Amp through the OUT-
PUT jack. Set TREPPIGO to UP & DOWN or to DOWN. If necessary, HOLD should be turned OFF to silence the unneeded channel.

8-4. KYBD GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)
Patch Number: B4
Test Mode: UP
Control: KYBD = 10

Note: WIDTH VR3 of CH1 (CPU BOARD) should not be set too close to FCW or FCOW position.

(1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
(2) Press C6 key and adjust KYBD GAIN VR10 (PANEL BOARD A) for 992Hz (B9 note).

8-5. WIDTH

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

Test Point: TP4 pins 2–6 (CH2–CH6) (CPU BOARD)
Patch Number: B4
Test Mode: UP
Control: KYBD = 10

Connect either Tuner or frequency counter to TP4 pin 2 (CH2).
Press C8 key and adjust WIDTH VR3 of CH2 (CPU BOARD) for 992Hz.
Repeat steps (1) and (2) for TP4 pins 3–6 (CH3–CH6).

8-6. VCF LFO OFFSET

Test Point: OUTPUT
Patch Number: B3

(1) Hold any key down.
(2) Quickly slide LFO up and down and adjust VCF LFO OFFSET VR8 (PANEL BOARD A) so that the pitch does not vary.

8-7. VCF LFO GAIN

Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)
Patch Number: B3

With LFO TRIG pressed, adjust VCF LFO GAIN VR8 (PANEL BOARD A) for 6Vp-p.
Note: When observed at the OUTPUT jack, the frequency should vary between 45–50Hz and 4–5kHz.

8-8. VCF ENV OFFSET

Test Point: OUTPUT or TP4 (CPU BOARD)
Patch Number: B3
Controls: VCA ENV/GATE = GATE ENVGS = 0
(Refer to "Edit Mode" section.)

(1) Press any key.
(2) Quickly slide ENV (VCF) up and down and adjust VCF ENV OFFSET VR13 (PANEL BOARD A) so that the frequency does not vary.

Note: When TP4 is used as the test point, adjust VR13 so that the waveform is stable, or without jitter.

8-9. VCF ENV GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)
Patch Number: B3

Press any key and adjust VCF ENV GAIN VR12 (PANEL BOARD A) for approx. 30kHz, IT = approx. 34us. (Fig. 35)

F 35

\[ T = 34us \]

9. PWM (CPU BOARD/PANEL BOARD A)

Note: Before this adjustment, the Sawtooth Adjustment must have been completed.

9-1. PWM 50%

Test Point: TP4 pins 1–6 (CH1–CH6) (CPU BOARD)
Patch Number: B2
Test Mode: UP

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press C4 key and adjust PWM 50% VR6 (PANEL BOARD A) so that duty ratio of pulse is 50% (Fig. 36).

Note: When observed at the OUTPUT jack, the frequency should vary between 45–50Hz and 4–5kHz.

9-2. PWM 95%

Test Point: TP4 CH1 (CPU BOARD)
Patch Number: B5

(1) Connect oscilloscope to TP4 pin 1 (CH1).
(2) Press C4 key and adjust PWM 95% VR7 (PANEL BOARD A) so that duty ratio is 95%. (Fig. 37)

Fig. 37

502 / 1002

505 / 1002

95%
10. ENVELOPE (CPU BOARD)

Test Points: TP6 pin 1 and TP7
Patch Number: 88
Test Mode: UP

(1) Disconnect 10P- and 5P-connectors (connected to ports WR through RESET) on rightmost side of CPU BOARD.
(2) Connect oscilloscope (2V/cm, 0.5s/cm) to TP6 pin 1.
(3) Adjust ENV TIME VR6 of CH1 for 3-second attack time from pressing of key. (Fig. 38)

Note: CHORUSBORD is located under BENDER BOARD.

Test Points: TP1 TP2

Fig. 38

(4) Reconnect oscilloscope to TP7. Reset oscilloscope time base to 50μs/cm.
(5) Holding down any key will display six growing waves on oscilloscope; CH1 being at leftmost position. Align rise time of remaining waves to CH1 rise time (coincidental max. to 0 transitions is desired.) (Fig. 39)

Controls: MANUAL = ON
VCA LEVEL = Approx. 0
CHORUS = 1

(1) Feed test signal (5Vp-p, 1kHz, SINE) to TP8 (CPU BOARD).
(2) Connect oscilloscope to TP1.
(3) Adjust BIAS VR1 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

Note: After adjustment, reconnect the connectors.

(4) Reconnect oscilloscope to TP2.
(5) Adjust BIAS VR2 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

Fig. 39

V(μ)

3s

H

Fig. 40

POWER SWITCH
13149101 WEAZA4
or
14149110 1801-0121

PUSH SWITCHES (without button)
13129321 SUTIIA-1 momentary
13129322 SUTIIA-2 maintained
13169605 KEJ1090 DCO, MEMO, TAPE, CHORUS

LEVER SWITCHES
13139136 SLE-622-18P DPDT
13139135 SLE-622-18P DPDT

SLIDE SWITCHES
13159352 HSV037-01-520 MEMORY PROTECT
13159550 EVA-AC314AGA HFQ FREQ

KEY SWITCH UNITS (LFO, TRIG)
(See p. 13 for detail.)
13129717 KEH1003 ass'y
13129714 KEH1003 switch proper
13129719 CHC32801A guide pin
22209208 CR8202A rubber cushion
12479703 KT3-2 key top

CASES
08197801 Cabinet
08380852 Side panel (right)
08380533 Side panel (left)
07285132 Top panel
07285111 Bender panel
0648184 Holder Black
or
0648164 Nickel
0658121A LED Display window
Rubber foot G-5

KNOBS, BUTTONS
22470128 Knob (VOLUME)
01680029 Knob (slide Pot, SW)
01680309 Button(orange) SUTIIA-1/2
01680308 Button(yellow) SUTIIA-1/2
01680306 Button(white) SUTIIA-1/2
01680307 Button(orange) KEJ1090
01680306 Button(yellow) KEJ1090
0168043 Button(gray) KEJ1090
0168044 Button(white) KEJ1090
Key top (ivory) KT3-2
(See KEY SWITCH UNITS.)

PCBs
1498161C CPU BOARD OPH161C
1498187C PANEL BOARD A OPH187C
1498188C PANEL BOARD B OPH188C
1498194A LED BOARD A OPH194A
1498162A BENDER BOARD OPH162A
1498189A CHORUS BOARD OPH189A
1498190A JACK BOARD OPH190A
1468094B POWER SUPPLY BOARD PSH094B
1468095B POWER SUPPLY BOARD PSH095B
1468092A FUSE BOARD PSH092A
1468093A FUSE BOARD PSH093A
15280412A FUSE BOARD PSH094A

JACKS
13449708 ELJ0522-01-10(twin, mono)
13449724 HLU2312-01-20 (stereo)

CONNECTORS
13436111 37-4016-R
1468094B DCR (connector) socket 0128026 5714S DCR connector cap
12559331 GGS-0.8A pri.(100/117V)
12559511 CEE 7500mA pri.(220/240V)
12559513 CEE T1.0A sec.(220/240V)

FUSES
1468094B DCR (connector) socket 020-022 PB-4 or PB-8 (compatible)

POSISTORS
15236899 ERS-B33561 560
15236910 ERS-B33512 1.2k

RESISTOR ARRAYS
13829821 RGSD 8 x 10k 10k x 8
13910113 RGSD 4 x 10k 10k x 4
13910114 RGSD 4 x 22k 22k x 4
13910117 RGSD 8 x 33k 33k x 8
13910118 RGSD 8 x 68k or RGD16104G
Ladder Network
PARTS LIST

**POTENTIOMETERS**

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<td>EWH-OTAS1B14</td>
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**COIL**

| 022A0108 | S16799 | 37μH |

**POWER TRANSFORMER**

| 022B057 | (100/117/220/240V) |

**DIODES**

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<td>15029169</td>
<td>KV1226-X or Y (varicap)</td>
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<td>15029411</td>
<td>LT-8001P (LED) used as a zener</td>
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<th>LN5268A (LED) display</th>
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<tr>
<td>15029410</td>
<td>LB620V2A (LED) display</td>
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**TRANSISTORS**

| 151591150 | 2CB934-0 or Y |
| 151591197 | 2SD880-0 or Y |
| 151591191 | 2BAI015-GR or Y |
| 151591207 | 2SA1124, 2SA1125-GR or Y |
| 151591217 | 2SC1923-0 or Y |
| 151591228 | 2SC752-G or 0 |
| 151591214 | 2SC1815-GR or Y |
| 151591227 | 2SC4215-GR or Y |
| 151591303 | 2SC638-0-F or Y |
| 151591080A | 2SC945 SELECTED FOR NOISE |
| 1515919601 | 2SB605-0 (3) |
| 151591260 | 2SD571-1 |
| 151591230 | 2SK30A-GR or Y (FET) |
| 151591236 | 2SC2878-A or B |

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**KEYBOARD**

| 004A0908 | SK-36IC (61 keys) |

**KEYBOARD PARTS**

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<tr>
<td>12569111</td>
<td>CR-1/3V 3V Lithium battery</td>
</tr>
</tbody>
</table>

**CAPACITORS**

| 1365922890 | EC95835S32SW | 3300μF/35V |
| 1365922890 | EC95835S25SW | 680μF/25V |
| 13589641 | ECO-114A73MR | 0.047μF |

**ICs**

| 151591150 | TC4066B |
| 151591160 | Quad Analog Switch |
| 151591017 | TC4069UB |
| 151591090 | Hex Inverter |
| 151591120 | Quad Analog Switch |
| 151591130 | TC4017AB |
| 151591120 | Hex D-type Flip-Flop |
| 151691120 | 7407 or 74S207P |
| 15169351 | Hex Buffers/Drivers |
| 15169341 | 74LS14 |
| 15169310 | Hex Schmitt Trigger Inverters |
| 15169312 | 74LS42 |
| 151692125 | BCD-to-Decimal Decoder |
| 15169119 | 7-Segment Driver |
| 15169112 | TL062CP |
| 15169112 | OP Ampl |
| 15169112 | BA1702PS/NUJ002D |
| 15169112 | HP5082C or TL082CP |
| 15169112 | OP Ampl |
| 15169112 | NJM952S |
| 15169112 | J FET Input Dual OP Ampl |
| 15169112 | NJM311D or PC011C |
| 15169112 | Voltage Comparators |
| 15169136 | MS218L |
| 15169142 | OP Ampl |
| 15169158 | TA7558S |
| 15169158 | OP Ampl |
| 15169158 | PC4538C |
| 15169141 | OP Ampl |
| 15169138 | IR3109 |
| 15169138 | VCF |
| 15169138 | IR301 |
| 15169138 | AB662A |
| 15169138 | VCA |
| 15169138 | TA75595 |
| 15169138 | Dual 0P Ampl |
| 15169138 | NJM3009 |
| 15169138 | BBD |
| 15169138 | MN3101 |
| 15169138 | BBD Driver |
| 15169141 | PC12522 (CYA) |
| 15169141 | AN7805 |
| 1516911100 | Dual Voltage Regulator |
| 1516911100 | 15V Voltage Regulator |

**ICs**

| 13589641 | Single 8ch Multiplexer |
| 13589641 | 80114A73MR | 0.047μF |