PARTS LIST

CASE
2202020500 Button cover
2219031801 PCB holder
2219031900 LED holder
2219032000 Switch holder
2219050900 Rack angle
2221031200 Control panel
2221031400 Rear panel
2222022903 Top cover
228032000 Chassis
2221071400 Display panel
2222031100 Control panel
2222031300 Rear panel
2220204003 Top cover
2281031900 Chassis
2221071300 Display panel
15029709 Fluorescent display FIPSAG8
15029710 Fluorescent display FIP16A8R

KNOB, BUTTON
2247039000 Knob 10mm dia.
2247025900 Knob ORN
2247026000 Knob GRN
2247026100 Knob YEL
2247026200 Knob BLK
22470514 Button WHT
2247024000 Button BLK
2247090300 Button Assembly (includes the following)
2218032000 Switch holder
2247053500 Button 1
2247053600 Button 2
2247053700 Button 3
2247053800 Button 4
2247054000 Button FEEDBACK
2247054100 Button TIME X2
2247054200 Button MOD
2247054300 Button DELAY PHASE
2247054500 Button TIME
2247090200 Button Assembly (includes the following)
2218032000 Switch holder
2247053400 Button BANK A/B
2247053500 Button 1
2247053600 Button 2
2247053700 Button 3
2247053800 Button 4
2247053900 Button FILTER
2247057700 Button FEEDBACK PHASE
2247054100 Button TIME X2
2247054200 Button MOD
2247054300 Button DELAY PHASE
2247054000 Button Assembly (includes the following)
2219032000 Switch holder
2247054400 Button FEEDBACK

SWITCH
1311201381 SUP-12
1152169211 KEF 10906
13130124 SUGA 3P
13129133 SUG-12
12421206 PRD-4

READ RELAY

JACK
13492328 HLJ3517-01-01
13492339 HLJ3517-01-03
13492440 HLJ3517-01-100

TRANSFORMER
2245034800 100/117V
2245034900 220/240V
2245035000 100/117V
2245035100 220/240V

COIL
2244023800 LPIF S097624
2244021900 LPIF S097623
12429236 OSC S097614 L1

PCB
7411606032 Main board (pcb 2291058201)
7411607001 LED board (pcb 2291058300)
7411608005 Switch board (pcb 2291058400)
7411609026 Main board (pcb 2291057901)
7411607001 LED board (pcb 2291058000)
7411608005 Switch board (pcb 2291058100)
7411609000 Power supply board (pcb 2291058500)
Fuses, Fuse labels, capacitor C1 excluded.
Specify model and line voltage when ordering for complete assy.
7411711002 RAM board (pcb 2291083000)
Analog SW board (pcb 2291091000)
Substitutive for HI-302 and HI-303.
No replaceable part. See P.20.

POTENTIOMETER
13219361 KO611008FE 100KB
13299101 EYT-R4S00B14 trimmer
**CAPACITOR**

| Code   | Value  | Brand    | Type   
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<thead>
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<th></th>
<th></th>
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<tbody>
<tr>
<td>13549884M0</td>
<td>0.01μF</td>
<td>Polypropylene</td>
<td>100V</td>
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<tr>
<td>13589455M0</td>
<td>0.01μF</td>
<td>Polypropylene</td>
<td>220/240V</td>
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<td>13589456M0</td>
<td>0.01μF</td>
<td>Polypropylene</td>
<td>117V</td>
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<td>13639154M0</td>
<td>100μF/F/16V</td>
<td>Electro</td>
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<tr>
<td>13639194M0</td>
<td>100μF/F/35V</td>
<td>Electro</td>
<td></td>
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<td>47μF/F/16V</td>
<td>Bi-polar, electro</td>
<td></td>
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<tr>
<td>13589139Y0</td>
<td>0.0012μF</td>
<td>Polypropylene ±1% (SDE-1000)</td>
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<tr>
<td>13589140Y0</td>
<td>0.0015μF</td>
<td>Polypropylene ±1% (SDE-1000)</td>
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<tr>
<td>13619703M0</td>
<td>0.22μF</td>
<td>A set of pair, selected (SDE-1000)</td>
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<tr>
<td>13639138Y0</td>
<td>0.001μF</td>
<td>Polypropylene ±1% (SDE-3000)</td>
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<tr>
<td>13619711M0</td>
<td>4.7μF/F/35V</td>
<td>Tantalum bead (SDE-3000)</td>
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<td>13639153M0</td>
<td>220μF/F/16V</td>
<td>Electro (SDE-3000)</td>
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<td>10μF/F/16V</td>
<td>Bi-polar, electro (SDE-3000)</td>
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**OTHERS**

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<tr>
<th>Code</th>
<th>Description</th>
<th>Code</th>
<th>Description</th>
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<td>12389718</td>
<td>FX-1 11.009kHz Xtal</td>
<td>2216032101</td>
<td>Insulation spacer (vinyl sheet)</td>
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<td>2216032701</td>
<td>Insulation sheet (fibre, L-shaped)</td>
<td>22160420700</td>
<td>Connection rod</td>
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<td>2215040100</td>
<td>Joint A</td>
<td>2215040200</td>
<td>Joint B</td>
</tr>
<tr>
<td>13439127</td>
<td>Connector housing 5045-11A 11P</td>
<td>13439157</td>
<td>Connector housing 5045-13A 13P</td>
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<td>2260143200</td>
<td>Connector wiring assy 11P</td>
<td>2260143300</td>
<td>Connector wiring assy 13P</td>
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<td>12569125</td>
<td>CR1/3N 3V Lithium Battery</td>
<td>2226022200</td>
<td>Cushion</td>
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<td>2225021001</td>
<td>Shield board (metal, L-shaped)</td>
<td>2225021100</td>
<td>Shield board (metal, flat)</td>
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<tr>
<td>2225021200</td>
<td>Shield sheet (foiled paper)</td>
<td>2216031300</td>
<td>Insulation spacer (vinyl chloride)</td>
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<td>13439120</td>
<td>Connector housing 5045-04A 4P</td>
<td>13439123</td>
<td>Connector housing 5045-07A 7P</td>
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<tr>
<td>13429143</td>
<td>Connector housing EMC-0760 7P</td>
<td>2341017100</td>
<td>Connector wiring assy 4P</td>
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<tr>
<td>2341018000</td>
<td>Connector wiring assy 7P</td>
<td>2341030700</td>
<td>Connector wiring assy 7P</td>
</tr>
<tr>
<td>2225021501</td>
<td>Shield board (metal, U-shaped)</td>
<td>13439125</td>
<td>Connector housing 5045-09A 9A</td>
</tr>
<tr>
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<td>Connector housing EMC0960 9P</td>
<td>2341043400</td>
<td>Connector wiring assy 9P</td>
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<td>2341030800</td>
<td>Connector wiring assy 9P</td>
<td>13439514</td>
<td>Connector PS-30 SD-5471-1 30P female</td>
</tr>
<tr>
<td>2341030900</td>
<td>Connector wiring assy 9P</td>
<td>13439516</td>
<td>Connector PS-30 FA-5471-A1 30P male</td>
</tr>
<tr>
<td>2341031000</td>
<td>Connector wiring assy 9P</td>
<td>2215009000</td>
<td>Spacer 13mm HEX threaded</td>
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<td>2341031100</td>
<td>Connector wiring assy 9P</td>
<td>13459123</td>
<td>GND terminal</td>
</tr>
<tr>
<td>12369511</td>
<td>Cord bushing BU4801</td>
<td>12369410</td>
<td>Line cord strain relief 1702B</td>
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CIRCUIT DESCRIPTIONS

General Description

SDE-1000/3000, Digital Delay Line, use RAM as memory device in which audio signals are stored by means of POM (Pulse Coded Modulation) method.

The delay unit first samples the input audio signal to have a series of discrete values of the signal amplitude at point. Each of sampled pulses is digitalized and stored into RAM cells as a binary coded data which, when a specified time passed, is read, restored to analog value, then injected into audio path as a delayed signal. The process can well be compared to that of conventional tape echo machine as shown in Fig. 1. RAM cells correspond to the tape and the RAM accessing to a Recorder/Playback head.

In operation R/P head first functions as a playback head and will read a group of RAM cells being in touch with, then quickly changes to a recording head to record digital data being fed from the A/D converter into the same cells. The head steps to the next cell group and repeats the read and write operations, then to the third, fourth and so on continuously until the time determined by DELAY TIME button comes. When the delay time has passed, the head leaves the remaining cells unused and jumps to the first cell group where it reads the previously stored data and writes the new data. The number of cell groups the head can see is based on DELAY TIME setting and the traveling speed of the head slows down one-half when in TIME X2 mode. In other words, the length of the tape varies with DELAY Time and the speed with DELAY Time Range (also X1—X1.5 setting and MOD rate).

The following description breaks major circuits down into Analog and Digital, starting with SDE-1000 circuits most of which are also found in SDE-3000, then goes through the circuits featuring SDE-3000. One major difference between two models are their time delay ranges: SDE-3000 four times the SDE-1000 in RAM memory capacity.

HEAD AMP

The Head Amp interfaces the unit with a variety of input signals so that the unit can operate with adequate signal to noise and without excessive limiting across the dynamic range of the signal. Although this amp has a gain range of 1 to 24, VR-6 (INPUT ATT) attenuates the delay signal as it is rotated from FCF position to CCW. The unit's overall gain is unity at FCF.

NOTE: Minor modifications are made on SDE-1000 head amp and associated circuits to provide more headroom without sacrificing tonal quality and sound level. Refer to Engineering Change in SDE-1000 section in this manual.

FEEDBACK/MIXING

The delay signal is mixed again with a new direct signal when 0V is placed on Q51 gate, and out of the delay line when –14V is on the gate.

PREEMPHASIS

This stage boosts higher frequency contents to provide a good S/N ratio. GAIN: unity at 1kHz and 2.5 at 10kHz.

LPF-1

An *Anti-aliasing filter including two filters of different cutoff point. Only one filter is connected to the next stage at a time. Passing TIME X2 switch causes the Control Logic (IC14, etc.) to place a ground to the gate of Q27 and –14V to Q28, limiting the filter’s output bandwidth within 10kHz — 8kHz. Disengaging the X2 switch conducts Q28 and cuts off Q27, extending the bandwidth to 17kHz. Control Logic also cuts off both FETs for 7 sec after power is first applied to the unit, and during HOLD ON mode or while Delay Time button is manipulated.

*Aliasing — The type of distortion that is found in "sampled" signal processing system when the signal has frequency components which exceed half the sampling frequency.

COMPRESSOR

This stage logarithmically reduces the dynamic range of the signal before it is digitalized.

NOTE: For detailed descriptions of S/H, A/D, D/A, Main Controller and RAM, see corresponding sections in SDE-3000 description.

SAMPLE & HOLD

ICs 5A and 6B, together with C13 extract a portion of the input signal at SAH rate. The sampled audio is fed through Q8 to pin 2 of IC2 where it is compared with 12 step voltages on pin 3 to have its analog voltage represented by digital code through A/D conversion.

NOTE: SAH rate is constant regardless of DELAY TIME setting, but varies when TIME X2, DELAY TIME X1/X1.5 or MODULATION is enabled.

A/D CONVERTER

The A/D Converter employed here is of Successive Approximation consisting of SAR (Successive Approximation Registers in IC12, Main Controller), IC3 and 4 which boost TTL compatible to 12V, VM-I ladder resistor which adds a corresponding analog weight to individual bit, Q8 and Q10 follower and comparator IC2. In operation, SAR first sets the highest bit (MSB) register to H (1) whose output is, after given the highest voltage at RM-1, compared with sampled audio at IC2 input. If MSB is larger than the sampled audio, it is reset to L01 by a H from IC2 (D IN).

If smaller, kept set and applied once more together with the second highest bit register output (H) that is one-half the highest in voltage. The process repeats for MSBs while the combination of SAR outputs is approaching to the sampled audio level. During the process, D IN is also transferred to RAMs IC9—IC11 to record H or L of all the bits which, when grouped into 12 bits, are the data of the sampled portion of audio input signal.
D/A CONVERTER
When the time determined by DELAY TIME has passed, some parts of A/D system serve as D/A converter. RAM stored 12 bit data is transferred in time sequence (3 bits parallel x 4 times) from each RAM OUT pin to IC12 where they are so arranged that they are fed simultaneously via D11-D10, ICs 3, 4, RM-1, Q9 and Q10 to S/H IC50 and IC51.

EXPANDER
One half IC15 NE570 exponentially amplifies delayed audio to restore it to the original dynamic range.

LPF-2
The configuration analogous to LPF-1, providing 18kHz bandwidth when O48 is ON, or 9.5kHz when O49 is selected by TIMEx2 switch. Being an Interpolating filter, it smoothes staircase-like out of the waveform. As just for LPF-1, mute signals are applied from Control Logic IC14.

DE-EMPHASIS
IC29 and associated components reduce higher frequency components in the delay line to compensate for preemphasis, restoring the overall frequency response to flat.

PHASE SELECTOR
O48, when conducted, change IC29 into an inverter, reversing the delay output phase with respect to the direct signal.

MAIN CONTROLLER
IC12 63H-101 a specially designed gate array for controlling digital delay system. It clocks most of delay related sequences such as A/D, D/A, S/H, RAM accessing, etc. in time with clocks generated at the internal timing generator which in turn is clocked on MSCK delivered from CLOCK Generator IC23. With TIME X2 button activated IC12 has an H on RNG1 pin and slows down all timing sequences by one-half except REFRESH cycle. The clock frequency can be varied by the external voltage to be applied on FC or PA.

As the name implies, IC12 Main Controller is the heart of the Delay Line. All the delay circuits will not work correctly should the Main Controller fail to receive adequate clocks from IC23.

IC12 PIN DESCRIPTION
SAH & RNG 1
SAH determines the rate of sampling being performed at IC5 which gates on a high SAH. When TIME X2 is engaged, RNG 1 turns from L to H, lengthening SAH intervals from 22.9µs to 45.8µs.

D IN
D IN accepts a series of H or L from the comparator IC2, resetting register(s) in SAR on H to omit it from the subsequent comparisons.

D OUT
These Hs and Ls on D IN are also transferred to RAMs (IC9-IC11) and stored as a set of 12-bit data which represent the amplitude of a portion of input signal (sampled audio) being fed to IC2 pin 2.

D0-D11
During A/D conversion cycle these pins represent comparison data from internal SAR. During D/A cycle, simultaneously output 12-bit RAM stored data which have been read from each RAM in time sequence (3 bits x 4) and temporarily buffered in internal three registers.

DATA & SHIFT (SIFT)
As mentioned in general description, RAM cells used for sound memory are varied with time delay. IC12 controls RAMs accessing sequence in accordance with DELAY TIME DATA received at SHIFT rate. The DATA is a serial stream of 16 bits and will change between:

- 16 bits
- MSB LS8
- 0000 0000 at 0ms setting and
- 0011 1111 at maximum setting
- 11 (SDR-3000)

The DATA/SHIFT are transmitted only after DELAY TIME or PRESET button is released.

The DATA is accompanied by several mute signals to cancel unwanted signals.

MUTE A: active low when DELAY TIME button is manipulated.
MUTE B: active low while PRESET is pressed.
To shorten the Mute periods, TIME X2, MOD, and X1.5 are disabled.

RS(RAS) 16
Falling edges of RAS (Row Address Strobe) enable each RAM to latch Row address (W/R cycle) or Refresh address into its designated cells.

CAS 1-CAS 3
RAMs IC9-IC11 latch Column addresses on negative edges of concurrent Column Address Strobe (CAS1CAS3) which also serve as Chip select, and read memory cell respectively. The data read are routed to the RAM D OUT (pin 14) while related CAS is low.
The frequency of Clock Generator is as follows (approx):
2.7MHz at Normal  1.7MHz at TIME X1.5
2.7M~3.3MHz at MOD max.  1.7M~2MHz at TIME X1.5/MOD max.

MSCK – Clocks the internal Timing Generator that times the most of digital circuits.

HDCk – The frequency of HDCk is MSCk or 43Hz at normal mode. Used by the CPU as a time base for calibrating Delay Time display. The CPU fails to read switches and it is HDCk period is outside
7m-50ms.

RAM 1—RAM 3

12 bit data read from three RAMs are fed through these pins to internal three shift registers for temporary storage. All the buffered bits are placed on D0-D11 at a time to form a 12 bit parallel data to be applied to D/A converter for reproducing a part of delay signal. During HOLD ON the A/D converter remains active but cannot receive input signal. The comparator output is inhibited from being written into RAMs.

TP-3
TP-1
5 µs/div

RAMs (IC9—IC11)

Record the results of Successive Approximation, from MSB (D11) to LSB (D0), sharing 12 bits – 4 specific bits for each as shown in the table at the beginning of General Description.

CONTROL SIGNALS IN DIFFERENT MODES

<table>
<thead>
<tr>
<th>MODE</th>
<th>MSCK</th>
<th>HSCk</th>
<th>AS</th>
<th>INDHV</th>
<th>IC1</th>
<th>IC2</th>
<th>AT</th>
<th>DELAY</th>
<th>DLYOFF</th>
<th>LEAD</th>
<th>HOLD</th>
<th>IC3</th>
<th>GATE</th>
<th>E</th>
<th>DQ8 GATE</th>
<th>C</th>
<th>DQ7 GATE</th>
<th>B</th>
<th>DQ6 GATE</th>
<th>A</th>
<th>DQ5 GATE</th>
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<td>1</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The CPU is provided with a battery backup to retain switch, delay time and preset settings.

Vcc : -4V < +3V (Pin 40) 3.3V
Vcc 5V (Pin 21) 0V
RESET 5V (Pin 4) 0V

POWER ON
Backup
Reset
Backup

T0 – Decides the operation mode of the CPU:
+5V – SDE-1000
0V – SDE-3000

T1 – Receives Clock pulses through IC12 HSCk pin. The clock serves as a time base to enable the CPU to calibrate Delay Time Display and is ignored by the CPU when Modulation is ON and MOD Foot control jack disengaged. (See HDCk, Main Controller.)
P20 (DATA) – Send memory access control data after every delay time
P21 (SHIFT) – settings (see DATA/SHIFT, Main Controller).
P23 – Becomes "L" for muting (See timing chart in DATA/SHIFT, Main Controller.)
P10 – Read SW1–SW10 through the matrix in combination with P24—
P11 P27 and DB7.
P12 – Input from PRESET SHIFT jack. A rising edge of this input stops PRESET memory.
P13 – MODULATION FOOT CONTROL jack input. With MODULATION ON and this input at low, CPU ignores T1 input. For example, rotation of DELAY TIME X1-X1.5 does not change TIME display.
P14 – HOLD jack input. When H. readings of TIME UP or DOWN and PRESET memory are inhibited.
P15 – PLAY MATE jack input. Active rising edge.
P16 – Rising edge from this pin latches the following logic codes made by DB8-DB3 into Analog Control IC17. TIME X2, DELAY PHASE, MOD and FEEDBACK
P24 – Output of switch scan signals which are read through P10 and P27.
DB7
DB6
DB5
DB8
DB8

DB9 – Besides Control signals for IC17, these pins deliver numerical data to fluorescent display via IC18 7-seg-decoder.
DB6: Dot Point signal.
DB4 – Send LED lighting signals.

NOTE: When P10, P11, P12 and P15 pins receive signals almost at the same time, the CPU gives priority to the signal first read. Example: PRESET SHIFT and Front Panel switches are disabled when PL+Y MATE has been activated.
The positive and negative peaks of a sampled signal are taken and detected at ICQ and IC7 respectively, resulting in a logic code as shown in the table below. The code is latched into IC33 at SAH rate, passes through IC34 (data selector) on "ll" DBS A/D cycle, and through ICQ 36C and D and reaches pins 6 and 9 of IC10 D/A attenuator. IC10 switches ON or OFF its analog gates to provide for correct D/A output level.

**CONTROL SIGNALS IN DIFFERENT MODES**

<table>
<thead>
<tr>
<th>Mode Operation</th>
<th>A 1</th>
<th>A 2</th>
<th>B 1</th>
<th>B 2</th>
<th>C 1</th>
<th>C 2</th>
<th>D 1</th>
<th>D 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mute</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
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<tr>
<td>0.5V</td>
<td>0 0</td>
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<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0.15V</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
<tr>
<td>0.1 V</td>
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<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

This logic code is also sent through IC33 to companding RAMs IC41 and IC43 while A/Ded input signal data is sent from comparator IC8 to RAM board via IC21. In other words, audio input is stored into two locations with different information—meter’s pointer deflection reading into IC10—IC12 on the RAM board, and meter range into companding RAMs.

**COMPARING RAMS (IC41 and 43)**

As shown in the Main Controller Timing Chart (see RAM1—RAM3) and RAM table, A/D data for a sampled signal is stored into RAMs (in the same R5 section) four times starting from MSB 3 bits (D11—D9).

On the contrary, companding data is stored into IC41 and IC43 once for the signal. However, since the same addresses are used for both RAM groups, companding RAMs cannot use the remaining three addresses if switch-able modification is made on them. IC31 issues address-offset data from DB0 and DB1 to IC28 and IC36 (Address Adder) which adds 0 to 3 at the memory banks change from RS16 to RS32, RS32 to RS46 and so on.

When in delay mode (D/A cycle, IC33 USBH+ and DB8=1), companding data is latched into IC32 on rising edge of DB4, selected by IC34 (pin 1=H), gated by IC35C and D, then routed to IC10. With this companding data applied IC10 determines the range of analog voltage from D/A converter IC16 and IC14, restoring RAMs (IC1—IC12) stored data to the original signal level.

**RAMS IC1—IC12 on RAM BOARD**

As mentioned earlier, during successive approximation of a sampled signal, comparison results are stored into three RAMs, being designated by RS, in 3 bits parallel X 4 serial format to represent the signal in 12 bit data. RAMs used for storing are always from those in RS16 IC12, 8 and 4 to RS64 (ICs 9, 5 and 1) depending on delay time settings. In short delay settings those RAMs of RS16 are repeatedly used while those in RS64 are left out of storing. This concept becomes important when troubleshooting RAMs. (Refer to the table on p.13).

**1. BRIEF CHECKING**

With relatively large signal applied to the unit’s input jack, observe TP1 (IC14 pin 6); Adjust the scope to display the waveform similar to that in the photo below.

Check steps of A/D cycle traces for 1/2-changes in voltage. If not, widely vary the input level and check whether companding circuit is ill affecting.

When A/D conversion seems defective, proceed to para. 5.

**2. DISCONNECTING COMPANDING CIRCUIT**

Companding circuit affects to both A/D and D/A converters. Disconnect the companding when checking the both circuits.

a. Disorder and remove the ground lead of R165 connecting to pin 6 of IC10.

b. Jumper wire across pin 6 of IC14 (TP1) and pin 2 of IC8 to bypass IC10.

If companding circuit seems defective, proceed to the next para.
SDE-3000 DESCRIPTION

The following sections concentrate to the circuits particular to SDE-3000. For other circuits not described, refer to those in SDE-1000.

HEAD AMP

Has a gain range of 2dB(1.26) to 30dB(31.6).

DELAY OUT/PHASE SELECT

This stage has 9.6dB gain. When TR78 is conducted, the delay out is 180° out of the direct signal.

MIXED OUT

Changes its gain with UNIGAIN settings:
- 7dB with UNIGAIN at +4dB
- 3dB with UNIGAIN at -20dB

CV IN

Level shifts 0 to +12V inputs to ±4V.

INV OUT

Level shifts ±4V inputs to 0 to +12V.

MOD DEPTH

Controls the amplitude of CV from CV IN or LFO with 0 to +6V coming via IC27A from RMB.

DATA COMPANDING

Audio signals are digitized with a 12-bit Analog to Digital Converter before stored into RAM. In ordinary D/A conversion, the number of significant digits decreases as input signal level decreases, lowering relative resolution. The reason is well illustrated by comparing A/D system to a voltmeter.

CV LINEARIZER

The output voltage at IC49A pin 1 is normally 0V. Has a unique voltage response curve to compensate for nonlinear V/C characteristic of D62 varicap in VCO circuit.

<table>
<thead>
<tr>
<th>MODULATION</th>
<th>X -- X1.5</th>
<th>IC49A Pin 1 (V)</th>
<th>VCO Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFF</td>
<td>X1</td>
<td>0</td>
<td>2.8</td>
</tr>
<tr>
<td>ON</td>
<td>X1</td>
<td>0 to -6</td>
<td>2.8 to 4.2</td>
</tr>
<tr>
<td></td>
<td>X1.5</td>
<td>+2.8</td>
<td>1.84</td>
</tr>
</tbody>
</table>

IC49A Pin 1 Output

MOD DEPTH: 50

IC31 MAIN CONTROLLER

DB0, DB1 Address offset data for companding RAMs.

DB4 Strobe. Latches data from companding RAMs into IC32 on rising edge.

DB5, DB6 Signals D/A or A/D cycle.

Cycle DB5 DB6 A/D L H

Suppose the voltages ranging from 1V to 100V are read with 100V scale, smaller voltages cannot be read accurately. The meter has to be switched down to lower ranges to allow the pointer stay around the middle of the scale. The same concept, named companding, is applied to SDE-3000 A/D conversion circuits.

The ideal companding system will work as follows:

With 100V, 10V and 1V input applied to the comparator (ICB) at different time, the D/A converter outputs the same successive voltages which are attenuated by IC10 by 1, 10 and 100 respectively before comparison. Consequently, the A/D converter has a higher resolution 100 times that of direct conversion at 1V input. The same procedure takes place, when RAM stored data are D/Aed as a delay signal, to correctly restore the voltage to the original level. Examples of companding effects are shown in the photos below. Note that waveforms at TP-1 will change drastically as the input varies in level, especially at a border of ranges where companding system works even for one waveform cycle of low frequencies. These phenomena should be made familiar to the eye of observer to avoid misjudging.
DIN of IC31
TP-1
Freeed from commanding effect.

3. COMPANDING CIRCUIT

When companding circuit seems malfunctioning, track the logic code from peak hold output to IC10 (see the table in “Peak Hold and Comparator” in the Circuit Description, SDE-3000). During a tracking the input signal must be set at a level for unchanged code. Then change input level for another logic code. Verify the identical code throughout A/D and D/A cycles. If a difference exists, check RAMs IC41 and IC43.

4. ISOLATING RAM GROUPs (RS16–RS64)

When delay time at which defective sound is reproduced is determined, it is easier to point out the RAM group containing the ill cell by referring to the table on the right. The DELAY DISPLAY can be a great help to measure the time when abnormal sound occurs on the border of two RAM groups.

a. With MODULATION OFF, set TIME to the maximum.

b. Adjust DELAY TIME (X1-X1.5) on the rear panel for 1600ms display.

c. With MODULATION DEPTH “0”, push MOD to ON.

d. Re-set TIME to around susceptible time. For example, if a noise pops closely at the middle of the delay time, set TIME for 200ms. If the noise disappears, failure may be located anywhere in a RAM of RS64.

5. ALL “1” & ALL “0” CHECKs

- Using sine wave as a test signal has adverse effects, that is, data in conversion system, RAM memory, etc. vary status from time to time as the input changes in level. When DC voltage at constant level is applied as an input signal, these data bits will stay at “1” or “0” at least for a certain period.

The waveform (and sound) will be disturbed at the moment when defective bit is reproduced. Check for jitter or glitch (pulse) at TP-1. If doubtful, proceed to para 6.

6. PINPOINTING DEFECTIVE RAM

Set DELAY TIME for 1600ms (see para. 4). Feed D IN of IC31 with +5V or 0V (para. 5). Connect scope to the bus of RAMs including suspective RAM. If the RAM is not defined yet, may have to be repeated for the other 2 buses.

For confirmation, first disconnect suspective RAM’s D OUT by cutting off the pattern to the bus, then observe the RAM D OUT directly.

Ideally, this can be accomplished by applying DC voltages (of max. or min. that can be accomodated by A/D system) to the input of the comparator IC8. Alternative to this is pulling up or down of D IN (IC31 pin 31):

a. Disconnect D42 cathode from TR97 (circuit dia. F-22).

b. A staircase “A” as shown in the figure will be seen at TP-1.

c. Connect a length of wire to D42 anode (or DIN of IC31) and touch the other end of the wire to ground point. A reversed waveform “B” will appear. D/A cycle is also inverted when the delay time comes; its amplitude being equal to that at the end of A/D cycle.
Earlier SDE-1000's have factory-modifications on INPUT Switch, Head Amp, Expander and Compressor as shown in the table below. The modifications add the following features (one by one) to the unit when it is used with UNIGAIN set in -20dBm.

- Greater Delay circuit headroom with better balance of Direct/Delay sounds in volume.
- Higher frequency response of the Delay line.
- Greater S/N ratio in Delay sound.

When need arises to implement one of the above to a given unit with serial number prior to 374800, the final values in the bottom of list should be applied since these improvements closely relate to each other. Exceptions are R271 and R272 which can be solely implemented for reducing noise from compressor.

**NOTE:** Changed parts are mounted in place on the parts side of the PCBs of 2291058202 and subsequent versions.

### PCB Version

<table>
<thead>
<tr>
<th>SERIAL No.</th>
<th>PCB Version</th>
<th>R39 (Ω)</th>
<th>R40 (Ω)</th>
<th>R41 (Ω)</th>
<th>R42 (Ω)</th>
<th>R45 (Ω)</th>
<th>R108 (Ω)</th>
<th>R145 (Ω)</th>
<th>R260 (Ω)</th>
<th>R271 (Ω)</th>
<th>R272 (Ω)</th>
<th>R58 (Ω)</th>
<th>R61 (Ω)</th>
<th>R189 (Ω)</th>
<th>R224 (Ω)</th>
<th>C114 (F)</th>
<th>C124 (F)</th>
<th>C48 (F)</th>
<th>MAX. INPUT LEVEL before clipping</th>
<th>INPUT -20dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>320100</td>
<td>320699</td>
<td>56K</td>
<td>18K</td>
<td>6K</td>
<td>6.8K</td>
<td>180K</td>
<td>3.3K</td>
<td>15K</td>
<td>33K</td>
<td>47K</td>
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<td>F</td>
<td>680</td>
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<td>F</td>
<td>-3dBm</td>
<td>HIGH 560KΩ</td>
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<tr>
<td>374800</td>
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<td>3.9K</td>
<td>68K</td>
<td>220K</td>
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<td>100P</td>
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<td></td>
<td></td>
<td>F</td>
<td>-3dBm</td>
<td>HIGH 560KΩ</td>
</tr>
</tbody>
</table>

**LOCATIONS**

- R39, R42(SW1A)
- R45(SW1B)/R108(IC8)/R224, C114(Q55)
- C124(VR6-SW1A)
- R40(SW1C)/R145, R272(IC15 pin 6)/R271(IC16 pin 12)
- C48(Q13-Q18)
- R189(IC20 pin 2)/R260(Q57)/R58, R61(Q18-JK3)

Cut pattern here and bridge with 1k (R272)
1. LEVEL METER CALIBRATION

1-1. Set UNIGAIN (rear panel) to ~20dBm.
1-2. Connect audio generator (AG) to INPUT jack and set AG for ~20dBm, 1kHz, sine.

1-3. Set RT8 at the point where +3dB LED just completely fades out.

2. DELAY TIME

2-1. Set DELAY TIME (VR1, rear panel) to X1.
2-2. Press and hold DELAY TIME button until DELAY TIME display reads maximum value.

2-3. Adjust RT6 for 379 ± 1ms reading.
2-4. Repeat step 2-2. If the reading changes, readjust RT6 for 379 ± 1ms.

3. COMPRESSOR LEVEL LINEARITY

3-1. Set DELAY TIME (rear panel) to X1 and UNIGAIN to ~20dBm.
3-2. Connect AG to INPUT jack and set for ~10dBm, 1kHz, sine.
3-3. Adjust COMPRESSOR OUT (VR4) for ~20dBm reading.

3-4. Reset AG to ~60dBm. Adjust RT1 for ~60 ± 0.5dBm reading.
3-5. VR4 and RT1 interact. Repeat from 3-2 through 3-4.

4. COMPRESSOR TOTAL HARMONIC DISTORTION

TEST POINT: TP2 (connect to oscilloscope - DC coupling)
4-1. Set DELAY TIME to X1 and UNIGAIN to ~20 dBm.
4-2. Connect AG to INPUT jack and set for 1kHz, sine, burst tone (4-0-4 cycles). Adjust AG output level so that the bottom (a) is at +1V on the scope.

4-3. Adjust RT2 for straight DC level.
4-4. Set scope V IN to AC coupling.
4-5. Repeatedly rotating INPUT ATT over its full travel, fine adjust RT2 for minimum DC drift.

5. EXPANDER TOTAL HARMONIC DISTORTION

TEST POINT: DELAY OUT (connect to scope - DC coupling)
5-1. Set DELAY TIME to X1 and UNIGAIN to ~20dBm.
5-2. Feed the same signal as for 4-2.
5-3. Adjust RT7 for straight DC line.
5-4. Set scope V IN to AC coupling.
5-5. Repeatedly rotating INPUT ATT over its full travel, fine adjust RT3 for minimum DC drift.

5-6. Connect amplifier/speaker to DELAY OUT and check for pop or rumble noise. If noticeable, check for absence of R71 and R722 (see table on the facing page) which are effective to the problem.

6. FREQUENCY RESPONSE

TEST POINT: DELAY OUT (connect to AC voltmeter)
6-1. Set DELAY TIME to X1 and UNIGAIN to ~20 dBm.
6-2. Connect AG to INPUT jack and set AG output for ~20dBm, 1kHz, sine.
6-3. Adjust INPUT ATT for ~30dBm reading.
6-4. Reset AG to 8.5kHz. Adjust RT4 for ~30.2dBm reading.
6-5. Press DELAY TIME X2 (ON). Reset AG to 400Hz, ~30dBm.
6-6. Adjust INPUT ATT for ~30dBm reading.
6-7. Reset AG to 5kHz, ~30dBm. Adjust VR5 for ~30.2dBm reading.

7. FEEDBACK

TEST POINT: DELAY OUT (connect to scope)
7-1. Set DELAY TIME to X1 and UNIGAIN to ~20 dBm.
7-2. Apply a signal (e.g., ~30dBm, 1kHz, sine) to INPUT jack for an instant and adjust RT7 for continual repeats at a level.
7-3. Verify decaying repeats with FEEDBACK at 7.5.
SDE-3000 ADJUSTMENT

1. VOLTAGES CHECK

2. INPUT LEVEL METER

3. VCO

4. LFO RATE

5. FREQUENCY RESPONSE

6. FEEDBACK

7. DIA OFFSET

ANALOG SWITCH BOARD 2291091900

Temporarily used for SN 372960-365099

--- Substitutes for ICS HI-302 and ICS HI-303 ---

Analog Switch Board 2291091900 is equivalent to HI-303 and HI-302 in operation and is installed on some units because of IC procurement problems. When the PCB needs replacing, use regular ICS for ICS and ICS10 respectively.

--- ohne 303 ---

--- without 303 ---
**EXAMPLES OF RAM FAILURE**
—No data on one RAM pin of Main Controller—

### SDE-1000

<table>
<thead>
<tr>
<th>INPUT</th>
<th>RAM1 (IC11)</th>
<th>RAM2 (IC10)</th>
<th>RAM3 (IC9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18dBm 1kHz</td>
<td><img src="image1" alt="Waveform" /></td>
<td><img src="image2" alt="Waveform" /></td>
<td><img src="image3" alt="Waveform" /></td>
</tr>
</tbody>
</table>

- **TP-3**
  - 5V/div
- **IC16 pin6**
  - 2V/div
  - 0.2ms/div

### SDE-3000

<table>
<thead>
<tr>
<th>INPUT</th>
<th>RAM1</th>
<th>RAM2</th>
<th>RAM3</th>
</tr>
</thead>
<tbody>
<tr>
<td>10dBm 1kHz</td>
<td><img src="image4" alt="Waveform" /></td>
<td><img src="image5" alt="Waveform" /></td>
<td><img src="image6" alt="Waveform" /></td>
</tr>
</tbody>
</table>

- **TP-1**
  - 20V/div
  - 5μs/div
- **TR45/TR50**
  - Emitter
  - 0.2ms/div
- **TP-2**
  - 5μs/div