**SPECIFICATIONS**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td></td>
</tr>
<tr>
<td>Level</td>
<td>+4 dBm (+29 dBm max)</td>
</tr>
<tr>
<td></td>
<td>-20 dBm (+5 dBm max)</td>
</tr>
<tr>
<td>Impedance</td>
<td>56kΩ</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td></td>
</tr>
<tr>
<td>Level</td>
<td>+4 dBm (+18 dBm max) into 600Ω load</td>
</tr>
<tr>
<td></td>
<td>-20 dBm (-8 dBm max) into 10kΩ load</td>
</tr>
<tr>
<td>Impedance</td>
<td>100Ω at +4 dBm position</td>
</tr>
<tr>
<td></td>
<td>850Ω at -20 dBm position, Mixed</td>
</tr>
<tr>
<td></td>
<td>550Ω at -20 dBm position, Delay</td>
</tr>
<tr>
<td><strong>Feedback</strong></td>
<td></td>
</tr>
<tr>
<td>Send</td>
<td>Level : +4 dBm (+16 dBm max)</td>
</tr>
<tr>
<td></td>
<td>Impedance : 100Ω</td>
</tr>
<tr>
<td>Return</td>
<td>Level : +4 dBm (+19 dBm max)</td>
</tr>
<tr>
<td></td>
<td>Impedance : 78Ω</td>
</tr>
<tr>
<td><strong>CV In</strong></td>
<td></td>
</tr>
<tr>
<td>Modulation CV</td>
<td>Operation Voltage : 0 to +10V (+20V, allowable)</td>
</tr>
<tr>
<td></td>
<td>Impedance : 90Ω</td>
</tr>
<tr>
<td><strong>General Performance</strong></td>
<td></td>
</tr>
<tr>
<td>Delay Time</td>
<td>0 to 320 ms</td>
</tr>
<tr>
<td></td>
<td>0 to 640 ms (in 1 ms steps)</td>
</tr>
<tr>
<td>Delay Accuracy</td>
<td>±0.5%</td>
</tr>
<tr>
<td>Frequency Response</td>
<td>10 Hz to 100 kHz</td>
</tr>
<tr>
<td></td>
<td>+0, -1 dB at Direct</td>
</tr>
<tr>
<td></td>
<td>10 Hz to 16 kHz</td>
</tr>
<tr>
<td></td>
<td>+0.5, -3 dB at Delay, 0 to 320 ms</td>
</tr>
<tr>
<td></td>
<td>10 Hz to 7.2 kHz</td>
</tr>
<tr>
<td></td>
<td>+0.5, -3 dB at Delay, 0 to 640 ms</td>
</tr>
<tr>
<td>Signal to Noise Ratio (IHF A) at rated input &amp; output</td>
<td>90 dB, Direct</td>
</tr>
<tr>
<td></td>
<td>90 dB, Delay</td>
</tr>
<tr>
<td>Dynamic Range (IHF A)</td>
<td>Greater than 112 dB, Direct</td>
</tr>
<tr>
<td></td>
<td>90 dB, Delay</td>
</tr>
<tr>
<td>Total Harmonic Distortion at rated input &amp; output Ref, 1 kHz</td>
<td>Less than 0.05%, Direct</td>
</tr>
<tr>
<td></td>
<td>0.08% typ, 0.2% max, Delay</td>
</tr>
</tbody>
</table>

**Am25L04**

Low-Power, Twelve-Bit Successive Approximation Registers

**LOGIC DIAGRAMS**

*The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. The device accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output (and the DO output) when the clock goes from LOW-to-HIGH. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration. The register is reset by holding the S (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state Q11 LOW, and all the remaining register outputs HIGH. The CC (Conversion Complete) signal is also set HIGH at this time. After the clock has gone HIGH resetting the register, the S signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q11 register bit and the Q10 register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the Q10 register bit and Q9 is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the CC signal goes LOW, and the register is inhibited from further change until reset by a Start-signal.*
SDE-2000 Brief Description of Operation

In ordinary delay and echo machines, device used to record sound information is mostly tape, BBD or CCD. Unlike these, however, the SDE-2000 employs the device of RAM. The recording method here is the one called the PCM (pulse-coded-modulation). In this, the sound signals are sampled at first, which then amplitude-converted to the digital form suitable for storing on RAM. The mechanism employed in this SDE-2000 for the signal delay system could easily be understood through comparison with that of the tape method, as follows. (See Fig. A)

- The medium which corresponds to the tape is a set of RAMs.
- Think that the heads rotates clockwise along the tape. The speed is reduced to 1/2 when the unit is set to "DELAY x 2" (position to mean the delay time is doubled).
- In the figure, the position (A) as pointed out by R.H. is the RAM write address and that of P.B.H. (C) is of the read address. The variable length (D) as being the difference of the two becomes the required delay time.

Note that, in this arrangement the position B is having more important meaning than D in handling the RAM addresses. The reason: The delay time which is firstly set on the Control Panel determines the address (B). With this B being added onto A, the address (C) is decided. On appearance, the read address (C) looks like rather in such a position as moving ahead. The fact is, the larger the value of B, the “shorter” becomes the delay time (D).
• The term of signal modulation through LFO or by means of external control voltage is in effect meant for just having the rotary speed of the heads varied in different degrees.

• Change in the head speed requires the corresponding changes on the access time to the memory cells and the duration of the signal being held on the heads (i.e. the time during which the read/write proceeds and the time for changing the data required on each -- packing density). To meet these requirements, all the logic circuits (including the "heads" and CPU) are being operated on timing given by the clocks generated in VCO. When VCO fails to generate, all these circuits also cease operation.

Q13, D1 and D8 make the thermocompensation circuit for KV-1 (Note: the varactor tends to vary its capacitance with changes in temperature).

Q15 is an AGC (automatic gain control). It functions to maintain VCO output amplitude constant through the frequency range.

Q12 is used to make the VCO's output level compatible with TTL.

Given these of the VCO clock timing, IC7 of the binary counter proceeds with execution of the program written on IC8. When the delay range, SW5C, is set to "DELAY x 2", the interval between the pulses adjacent to each other comes to be doubled.

When SW6B (DOWN) and/or SW7B (UP) are in the push-closed state, CPU is to output the delay time address with the length proportional to the time length of SW6B and/or SW7B being kept depressed.

CPU also outputs from the pins P25-P27 and D80-D83 the delay time display data, the product of an address as above multiplied by the time period between neighboring pulses applied from the Address Counter to the pin TI. These display data are then to be modified as follows in accordance with the status of the following two switches. Note that, during these operations, the delay address itself (B in Fig. A) is kept on as being set without any change.

• When SW5C is pushed in and placed at "DELAY x 2", the value of the data becomes halved (x 1/2).

• When JK10 is engaged and the associated jack switch becomes turned off (DB7 goes high), the display data will be changed successively in accordance with the change of the CV coming in onto EXT IN.

• If JK10 is left blank and MODULATION SW9 is placed at ON, the output from DB4 will become zero (0) and the DOT LED is turned OFF.

RAM ADDRESS

• RAM ADDRESS COUNTER (IC13, IC14):
  This address counter functions to increment the RAM address in synchronisation with the clock sent from IC7 of the Binary Counter.

• RAM READ ADDRESS ADDER (FULL ADDER) (IC12, IC16 — IC18):
  The adder performs the arithmetic operation to add the value of B onto the write address A so as to get the address value with which the RAM cells can be accessed on a delayed timing corresponding to D in Fig. A.

• ADDRESS SELECTOR (DATA SELECTOR) (IC15, IC19 — IC21):
  This is to select either the address A or A+B in accordance with the mode selected to either READ or WRITE.

• RAM ADDRESS MULTIPLEXER (IC23, IC24):
  Since µP416 is an RAM of 16K bits (16,384 = 2^14), a total 14-line address bus is required to make access to all of the memory cells.
  In µPD416, however, all cells are accessed by way of two addresses of ROW and COLUMN of 7 bits each. These addresses are output on a common bus on a time sharing basis in 2 times of 7 bits each.

CPU BORD

CLOCK GENERATOR

• LFO (IC2, IC3B):
  On Pin 1 of IC2A, square waves of 30V/p are produced. These waves are converted to triangle waves by IC2B, and again to sine waves through IC3B. When there is no external control (CV IN) applied, SW8 selects either one of these triangle or sine waves to transfer them through VR11 to the input pin 2 of IC1 on the CV LINEARIZER circuit.

• CV IN (JK10, IC3A):
  IC3A makes the input signals to be level shifted and expanded of the range, too. For instance, when external input (CV IN) is swinging from 0V to +10V, the voltage level to appear at the pin 1 is also being changed from -12V to +12V accordingly. When JK10, which incorporates a switch, is engaged, not only it works to disable the output of the LFO but also gives effect on the function of the delay time display circuit. More detail will be discussed when we come to the Display Circuit.

• CV LINEARIZER (IC1A, D3 — D6):
  The varactor (variable capacitance diode) KV-1 used on VCO (VCO will be discussed on the next paragraph) is the one having non-linear characteristics on its response to the applied voltage variation. The output of this CV LINEARIZER is therefore made to compensate it by having itself the curve that they both together can make a linear characteristic response.
  The FET switch Q7 functions to inhibit the modulation when a delay time is on the process of being set (SW6B and/or SW7A in off period).

• VCO (Q10 — Q15):
  Q10, Q11 and Q14 are the oscillation circuit. The frequency is under the control of the CV derived from Pin 7 of IC1. For instance:

  CV = +2V . . . 0.35 MHz  CV = ±10V . . . 1.56 MHz
  CV = -2V . . . 2.34 MHz
ANALOG TO DIGITAL CONVERTER

The A to D conversion used in the SDE-2000 is a variation of Successive Approximations (SA) comprising an A-D converter, comparator and successive approximation registers; its process is slightly different from the conventional method as follows.

* Negative logic D-A conversion
* Comparator does not compare D-A output directly with the input signal. It compares voltage difference between input signal and D-A output with the fixed (zero) voltage (see Fig. 3).

To avoid confusion, a brief review of common SA method is in order. In its simplest form, a conventional SA consists of a comparator, flip-flops and flip-flop set/reset control as shown in Fig. 1A.

![Fig. 1A](image)

INPUT +15V

D/A OUTPUT
0 1 1 1 1 = +15V

![Fig. 1B](image)

Assume that the system measures input voltages up to 31V with 5 bits, 1 bit/V resolution, for easier calculation. Initially, all FFs are reset, then FF4 is set which produces the most significant DC voltage (16V) at D4, which is in turn compared with input voltage (example, 15V). The comparator output goes low, resetting FF4. D4 goes 0 volts. FF3 is set in the same manner and delivers 8V at D3, exactly one-half the voltage of D4. The comparator output is high and FF3 remains set. Next, FF2 is set and total voltage (8V + 4V) from two FFs is now compared with the input voltage. The process is repeated for the remaining FFs. The state of the FFs after comparison against input voltage represents the digital value of the input signal. (Fig. 1B)

DUPLICATING THE PRECEDING PROCESS THROUGH A-D PORTION OF THE SDE-2000 CIRCUITRY

The voltage graph in Fig. 3A is an inverted image of Fig. 1B. When the most significant register in IC25 is set, it delivers low output (0 volts). Bits 01111 are sent via DATA SELECTOR to D-A converter IC3. With this data applied IO pin of IC3 draws from IC5 output the current which develops 16V across R87 (3K ohms). IO pin also draws from 5H output the current corresponding to inverted 01111 or 10000, causing voltage drop of 16V across R79 (3K ohms). The variation of currents at IO and IO pins is complementary, that is, the amount of current flowing into IC3 is always constant; when IO pin draws more current, IO pin decreases the same amount. (Differential Output Currents)

Voltage at (+) pin of IC2 becomes −1V (15V − 16V), changing its output to H, resetting D11 in IC25 − D11 changes from L to H. After all MSB 5 registers have been subtracted from input signal and tested against 0V, the configuration of registers will be 10000 = 16 (V). Why is 16V data proportional to 16V input? 16 volts is what will be developed across R87 and D-A output will be 31V − 16V = 15V.

Since comparator wants to know only relative voltage difference between the input pins, absolute voltage value is not necessary at (+) pin of IC2. Diodes keep the voltage range within diode drops (+0.6V).

NOTES:
In actual system, input signal ranges from 0V to 12V and is A-Ded with 12 bits, resolution is 12V/2^12, approximate 3mV. In this example MSB 5 bits only are used and input signal is 15V as before.

![Fig. 3A](image)

![Fig. 3B](image)

![Fig. 2](image)
APR.15, 1982

CPU BOARD GL4114-090 (7411409012)(pcb 2291050500)

DISPLAY BOARD
OP4114-130
(7411413002)
(pcb 2291050600)

LEVEL METER BOARD
OP4114-120
(7411412001)
(pcb 2291050700)

L1 SAMPLING CLK FREQ
M74LS393P
DUAL 4-BIT DECADE AND BINARY COUNTERS

Am27S19
256-Bit Generic Series Bipolar PROM

Three-state, standard 32 x 8 Schottky read only memory with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_6 - A_0$ and holding the chip select input, CS, at a logic LOW. If the chip select input goes to a logic HIGH, $O_0 - O_7$ go to the off or high impedance state.

Am6012
12-Bit High-Speed Multiplying D/A Converter

12-bit monotonicity
Differential current outputs
Differential nonlinearity $\pm 0.025\%$
Full scale current $4mA$

Ladder resistors connecting to 7 comparators provide reference voltages for each (+) input of comparators. The voltages are supplied from internal source and are in VU steps. When the voltage on (−) pin of a comparator exceeds (+) input, the comparator turns the constant current source on, enabling the LED to be driven.
EFFECT BOARD ET4114-060 (7411406010)(pcb 2291050402)

VR1 TP1 COMPRESSOR THD
VR2 COMPRESSOR LINEARITY
VR3 EXPANDER THD
VR10 LEVEL INDICATOR
VR5
VR6 LPF FREQ DELAY x 2
VR4 LPF FREQ DELAY x 1

PRIMARY FUSE BOARD
PS4114-141 (7411414100) 100V
PS4114-143 (7411414300) 117V
PS4114-144 (7411414400) 220/240V
 pcb 2291050800
**ADJUSTMENT**

**SAMPLING CLOCK FREQUENCY**

1. Turn power on 2-3 minutes before starting adjustments, for warmup.
2. DELAY on, DELAY x 2 on. While holding DELAY UP, push DOWN until the longest time is displayed.
3. Using non-magnetic (preferable) tool, adjust L1 on CPU board for 668-3 ms display.
4. Push DELAY x 2 (off) for the next adjustment.

**COMPRESSOR LEVEL LINEARITY**

1. Connect audio generator (AG) to INPUT jack and voltmeter (VTM) to DELAY OUTPUT jack.
2. Place UNIGAIN at +4dBm.
3. Set AG for +4/-0.2dBm, 1kHz, sine wave. Note the reading on VTM.
4. Reset AG for -30/-0.2dBm.
5. Adjust VR2 on Effect board for a VTM reading 40/40/-0.3dB below the reading noted at step 3.
6. Repeat step 2. Reading may differ from that has been. Repeat steps 2 thru 5 until no further adjustment is necessary.

**SDE-2000**

**COMPRESSOR TOTAL HARMONIC DISTORTION**

1. Place UNIGAIN at -20dBm.
2. Connect scope to TP-1 on Effect board. Set scope for AC couple, 2V/div, 1ms/div.
3. Connect AG to INPUT jack. Set for 1kHz, sine, burst tone (4 – 0 – 4 cycles); set the level for more or less clipping at peak 2.
4. Reset scope V for 0.1V/div.
5. Adjust VR2 so that DC level is straight.
6. While rotating INPUT VOLUME 0 – 10 – 0 repeatedly, adjust VR1 for minimum level drift on DC line.

**EXPANDER TOTAL HARMONIC DISTORTION**

1. Place UNIGAIN at -20dBm.
2. AG setting: Follow preceding paragraph.
3. Connect scope (DC couple, 1V/div, 1ms/div) to DELAY OUT jack.
4. Adjust VR3 for straight, drift-free DC line.
5. Reset scope for 2mV/div.
6. While rotating INPUT VOL 0 – 10 – 0 repeatedly, adjust VR3 so that DC line moves in parallel with horizontal line at VOL travel.
LPF FREQUENCY RESPONSE

DELAY x 1
1. Place UNIGAIN at +4dBm.
2. AG to INPUT jack; set for −20±0.1dBm, 1.4kHz, sine.
3. VTM to DELAY OUT jack; note the reading.
4. Reset AG for −20±0.1dBm, 14kHz, sine.
5. Adjust VR4 so that VTM reading is 0 to 0.3dB less than that noted at step 3.

DELAY x 2
1. Push DELAY x 2.
2. Reset AG for 1kHz, keep its output to the above mentioned level.
3. Note VTM reading.
4. Reset AG for 5kHz, keep the level constant.
5. Adjust VR5 so that VTM reading is 0 to 0.3dB less than that of step 3.

INPUT LEVEL INDICATOR

1. Place UNIGAIN at −20dBm.
2. AG to INPUT jack; set for −20dBm, 1kHz, sine.
3. Turn VR10 until INPUT 0dB segment lights up.

The RAS loads the row address and the CAS loads the column address. Both address signals share 7 input lines. Active cycles are initiated when RAS goes low, and standby mode is entered when RAS goes high. The three-state output buffer turns on when the column access time has elapsed and turns off after CAS goes high. Input and output data are the same polarity.