**SERVICE NOTES**

**SPECIFICATIONS**
- Rhythm storage capacity: 32 steps/measure, 64 measures x 12 tracks.
- Tempo variable range: 4M - 400
- Master output: Hi: 6V p-p/1KΩ, Lo: 0.6V p-p/3KΩ (Level: Voices @ red mark; AC @ FCW)
- Multi output: 1KΩ
- Trigger output: +15V, 20ms; 1KΩ -CB/PI/MA)/AC-
- Power consumption: 8W
- Dimensions: 508 (w) x 305 (d) x 110 (h) mm
- Net weight: 5kg

**CAUTION**
Although some parts are designated in abridged number or numberless in this limited space, there are fully numbered on the Parts List. Parts order must be written in full number followed by the part name to encourage prompt, accurate dispatch.

**TOP PANEL REMOVAL SCREWS:**
1. DUST COVER N-102
2. SWITCH SGM52-12P
3. KNOB N-128
4. SWITCH SWM-101C
5. BUTTON N-906 BLACK
6. PANEL N-142
7. SIDE PANEL N-118 (L)
8. KNOB N-128
9. SWITCH SGM120R
10. SWITCH DS1/2 188
11. KNOB N-165
12. POT, CARTRIDGE 18KΩ x 2
13. DUST COVER N-115
14. SWITCH XS1250
15. LED TLB124 RED
16. KNOB N-180 RED
17. KNOB N-168 ORANGE

**SCREWS:**
1. 3 x 6 mm B1, Fe, Br, Binding, Self tapping
2. 3 x 10 mm B1, Fe, Br, Binding, Self tapping
3. 3 x 10 mm B1, Fe, Br, Binding, Self tapping

**RUBBER FOOT 0.7 (111-073)**

**COIN SCREW 3 x 8mm**

**RUBBER FOOT 0.5 (111-021)**

**BATTERY COVER N-159**

**CUSHION N-310**

**DIN CONNECTOR T025B50103 (13429004)**

**SWITCH SGM24 (13189112)**
**General**

As can be seen from the block diagram, most processes of TR-808 up to generation of pulses triggering sound generators are controlled by the computer. CPU pin functions are as shown at the lower left table.

Once power is turned on for TR-808, pulses are generated from P1-2 of CPU regardless of TR-808 function mode (Start/Stop) and of presence or absence of rhythm patterns. The time length between the pulses is equal to that of the shortest rhythm pattern. The pulse is transferred to TRIGGER MONO, then ACCENT from which it is applied in parallel to all the gates prestaged to Sound Generators; accordingly, called COMMON TRIGGER. On the other hand, instrument data designating sound to be outputted are independently supplied to the gates from corresponding exclusive ports (PD, PE and PF1). Since Instrument data are time sharing the data bus with memory addresses, the data are aligned with Common Trigs in timing. When these two signals are applied, the gate ANDs the two signals and outputs a signal triggering the sound generator. Since the peak value of this trig is in proportion to that of the Common Trig pulses, when an accent data is outputted, the data can be used to change the amplitude of the Common Trig signal.

Panel control settings are read by interruption of CPU each time an interrupt signal is fed to the INT terminal. First, the Buffer & gate turns on by a signal from PH, and the status is read through PA. Then, some statuses of function switches are read through PB by a signal from one port of PH. At the same time, some statuses of a group of step switches are read through PB, and the step LED drive signal is outputted from PB as required. Statuses are read each time an INT signal is fed. However, statuses of the step and function switches are read every four times of INT signals.

Four CMOS RAMs (1K x 4-bit) are used for data storage. Chips are selected when the upper two bits of PE data decoded by ICE are enabled by pulses from P1-1. Addresses of memory cells are designated by bits of PO, PE and PF. Data storage to addresses is possible when an L output from P1-0 is applied to WE.

**Detail**

**SW Scanning, Status Reading**

Reading of statuses of the controls on the panel (step switches, function switches, tempo, etc.) starts when an interrupt signal is applied to INT terminal every 1.9ms. When the signal is applied to INT terminal, CPU starts interruption. The interruption period is approx. 600μs. During the first 150μs, PH0–PH3 become H, and the collector of AND gate Q18 becomes L. STATUS signals are ANDed with this L by IC3 and read through PA. After 150μs, only PH0 becomes L. This signal is converted to H by Q23, and reaches PB and PA through the closed contacts of the Step switches (No. 1–No. 4, SW1 (Model) and SW2 (Clear)). When one of the four Step switches is closed, the corresponding LED lighting signal is immediately fed from PG. Since the PG output is latched until the next INT signal is applied, the lighting period is approx. 1.8ms. This period b is approx. 450μs. The remaining period c is for processing of the main program. When the next INT signal is applied, PH0–PH3 become H again, the statuses of the TEMPO CLOCK, START/STOP, TAP, etc. are read again. Then, only PH1 becomes L and the statuses of switches connected to the collector of Q24 are read. At the next INT signal, STATUS and PH2 become L. Next, PH3 becomes L. This change is repeated. In this way statuses are checked each time an INT signal is applied every 1.9ms so that the CPU can respond to the status change promptly. The statuses of other switches are read every four times of INT signals. This corresponds to one reading every 7.6ms.
**RAM, Address Decoder**

Four static CMOS RAMs (µPD444C, 1K x 4-bit) are used for memory. The memory map is shown in Fig. 4.

The upper two bits PE2 and PE3 of CPU designate a RAM, IC5 decodes these bits, and the memory select is enabled by a signal from Pi-1 (CE). See Fig. 5.

Cell addresses are designated by bits from PD, PE, and PF. After 10µs of CE, the data shown in Fig. 5-2 is read (5-3) or a new data from PC is written (Fig. 5-5).

As can be seen from Fig. 5-2 and 4, during writing, PC output data and RAM data at the I/O ports of RAM may conflict with one another. To prevent this, the buffer resistors (R85-R88) are connected.

The LED driver transistors (Q2-Q5) for BASIC VARIATION, 1ST and 2ND are directly connected to the bus of PD and PE. However, since various data appear on the bus by time sharing processing, the LEDs may sometimes light even when unnecessary signals are applied, resulting in possible lighting timing disparity in a mode.

RAMs' low power consumption during high CE allows memories to be maintained for longer period with back-up battery.

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**Trigger Gate**

Pulses corresponding to the shortest rhythm step usable by TR-808 are fed from Pi-2 of CPU at a time interval determined by the setting of TEMPO CONTROL (Fig. 6-1). On the other hand, instrument data to be reproduced are applied from PD, PE, and PF to the gate of each sound generator in synchronization with step pulses (Fig. 6-3).

Since the step pulse width of 10µs is too narrow to trigger a sound generator, it is widened to approx. 1ms which is nearly equal to the width of instrument data signal. This widening is accomplished by the monostable IC6. It is triggered by a rising edge of Q27-inverted pulse. (Fig. 6-2). The L period is determined by the sum of the time constants of R100 x C23 and R102 x C27.

The output from pin 10 of IC6 passes through the ACCENT circuit composed of Q31-Q34, becomes a COMMON TRIG signal, and simultaneously applied to the gates of all sound generators in parallel. When instrument data is present at a gate, this trigger signal is ANDed with the data and activates the corresponding sound generator (See Fig. 7).

Since the AND output from the gate is in proportion to the amplitude of the common trig signal, the output of the sound generator has the amplitude in proportion to the common trig signal. Accordingly, when ACCENT data are present, they are added to the common trig signal. Since the output of pin 10 of IC6 is a negative logic signal, when there are no step pulses, the output signal becomes H, Q31 turns on and places a ground at base of Q32. When pin 10 of IC6 becomes L, Q31 becomes off, and when ACCENT data from PF-3 is L (no accent), Q34 turns on to shunt VR3. As a result, the base of Q32 becomes approx. +5V and trig amplitude is approx. 4V. When ACCENT data is H, a voltage between 5V and 15V according to VR3 setting is applied to the base of Q32, and is converted into trig pulses of approx. 4-14V. This explains that ACCENT level can be changed by VR3.

In the case of CB, CY, OH and CH, trig variation range is narrowed to 7V-14V by 1/2 IC2 (pins 1-3) on the voice board to increase S/N ratio.
START/STOP & Tempo Clock

When the power supply for TR-808 is turned on, the TEMPO clock continues oscillation regardless of the operation mode of TR-808. However, when the START button is pressed in the STOP mode, oscillation stops once for times to provide a mode change preparation time to CPU. In this way, the START/STOP circuit and the TEMPO circuit are closely related with each other. When the SYNC IN/OUT switch is set to IN, both circuits become ineffective and external signals from the DIN socket duplicate the both circuits.

When the START/STOP switch is pressed (closed) with rhythm stopped, Q of F-F (IC2B) becomes H, the collector of Q12 becomes H, Q of IC2B becomes H and IC2A is reset. Q of IC2A becomes H and the collector of Q12 becomes L. Then, since Q of IC2B becomes H, pin 2 of IC1 becomes L to turn on Q16. As a result, the TEMPO GENERATOR at 2/4 IC1 (D, E) stops oscillation (details are described later). After 9ms later, pin 1 of IC1A drops below the threshold level and pin 2 is reversed. The rising edge reverses Q of IC2A to L and the collector of Q16 (TEMPO CLOCK output) becomes H. At the same time, Q16 is cut off, and C10 starts discharging through the ANTI-LOG Q14 to continue oscillation. This discharging speed of C10 determines the oscillation frequency of the TEMPO clock. The variation range is between 8.3ms and 68ms. With TR-808, 1ms is defined to have 24 clocks, and thus 1ms is approximately equal to 400-300.

When the level of C10 exceeds the threshold level of pin 13 of IC1 due to discharging, the output of pin 10 is reversed, Q16 turns on, and C10 is charged. The output of pin 12 of IC1 is divided into 1/2 by T-F of IC2A.

FIGURE 8 START/STOP & TEMPO CLOCK CIRCUITS

FIGURE 9 TEMPO CLOCK TIMING DIAGRAM

FIGURE 10 POWER ON/OFF DETECTOR

Muting, Reset

The circuit composed of Q10–Q12 detects power on/off or sharp voltage drops in TR-808 DC lines and feeds forward bias (9 volts) to FET switches connected to point A. These FETs are for resetting CPU (Q64), preventing writing into RAM (Q75) and muting Master Out (Q13).

Power on: 0V to 15V
Power off: -15V to 0V

If this circuit is defective, the CPU may be kept reset. [Detail in TROUBLESHOOTING on page 14.]

FIGURE 11 REPRESENTATIVE BRIDGED T-NETWORK

FIGURE 12 REPRESENTATIVE SWING TYPE VCA

Sound Generators

The bridged T-network filter shown in Fig 11 is used to generate periodic damping drum sound. This configuration has variations according to application (instrument sound). Values of R and C can be changed. With this circuit, the decay time becomes longer as Q increases.

The swing type VCA shown in Fig 12 is used to generate metallic sound (noise). This circuit features its output waveform having many high harmonic components to provide ringing metallic sound. Major features of each sound generator are described below.

Bas Drum

This sound generator is composed of a multi-feedback, bridged T-network including 1/2 IC12 (pins 1–3) as an active element. The decay time of the resonating waveforms can be controlled by adjusting feedback amount by VR6.

Immediately after a trigger pulse is fed into the generator, the filter's time constant—in which the output is taken—halves and has a resonance on twice its inherent frequency for a half cycle period, then on the fixed frequency with decaying amplitude. This changing frequencies will sound a pungent crisp bass. This trick is performed by the circuit composed of Q41–Q43.

When a trigger signal is outputted from the collector of Q40, Q41 turns on, Q42 turns off, Q43 turns on and R166 is shortened. This halves the time constant of this network. The ON period of Q43 is determined by R166 and C38 and equals 4ms which is 1/2 x 1/2 of 16ms of the inherent oscillation period of the filter. When Q42 turns on after 4ms, current discharging from C38 via R161 produces a refrigeration pulse. At this time the generator oscillates on the inherent frequency.
Snare Drum
This sound generator has two bridged T-networks for fundamental waveforms and harmonic waveforms. The output ratio of the two can be changed by VR8 to tailor sound characteristic. The amplitude of snappy envelope can be controlled by VR9.

LT/LC (MT/MC, HT/HC)
These three sound generators are composed of the circuits based on the same principle. LT/LC is described below as an example.

This sound generator is composed of a multi-feedback, bridged T-network including IC5 as an active element. Voices are switched by SWB (C77 – frequency, R224 – level). While the oscillation is large in amplitude immediately after triggering, it is on a higher frequency due to conductors of D80 and D81, which reduce time constant of the filter. As the resonance is damped, its frequency is lowered by the effect of increasing diodes' internal resistance. Timbre variations corresponding to time elapse will appreciably be heard as in the case of Bass Drum.

Pink noise with a slightly longer decay time is mixed for Low Tom Tom to provide artificial reverberation.

RS/CL
CL Output from multifeedback bridged T-network incorporated with IC20 is routed to IC19. Output from IC21 (for R5), also routed via R320, can be ignored because of its minimized level due to impedance imbalance at pin 7 of IC20.

RS Disconnected R313 makes IC20b just as a buffer for C120a output. The output of IC20b is applied to O62 together with the output of IC21. The envelope applied to O62 is formed by R107 and C24. As described in the beginning of this section, VCA of this type is intended to provide many high harmonics in the output signals. Normally-conducting Q74 remains off only while trigger pulse is transferred from O61 to allow IC19 to pass signals. This switching is provided to eliminate noise leaking from IC20, especially for CL – relatively large amount, being wired for high Q.

CP/MA
White noise passed through the band pass filter (IC21) is applied to two VCAcs in parallel to have different envelopes. These envelopes are combined to obtain sound source for the CP sound generator.

Since an envelope with a relatively long decay time is applied to the VCA Q70, output from this VCA constitutes reverberation of CP sound.

The output envelope at the VCA (IC22, Q71 and Q72) is a unique sawtooth shape, and is a main component of this sound generator. The sawtooth envelop generator circuit is mainly described below to explain its rather complicated operation. When trigger pulses are applied to pin 8 of the quad comparator IC23, the output is integrated by R350 and C140, and converted into pulses of 30ms wide as shown in Fig. 13-2. At the falling edge of the pulse, pin 13 of IC23 becomes H (Fig. 13-3). The output from pin 1 of IC23 is also applied to pin 4 of IC23, pin 2 of IC23 becomes from –15V to 0V.

![FIGURE 13 HAND CLAP GENERATING CYCLE](image)

Q73 turns on, pin 5 of IC23 becomes –15V, pin 2 of IC23 returns to –15V, and Q73 returns to off state. Accordingly, the output waveform at pin 2 of IC23 becomes narrow pulses as shown in Fig. 13-5. The moment Q73 is turned on, C144 is abruptly charged to –15V. However, immediately, O73 turns off and the charges are discharged through R365 and D71. When the level of pin 5 of IC23 becomes higher than the level of pin 4 due to discharging, pin 2 of IC23 reverses again and C144 is recharged to –15V. After this process is repeated and advanced to the middle of the third time, pin 1 of IC23 rises to 0V. This signal is differentiated by R357 and C141, and the generated pulse turns on Q73. At this time, although the terminal voltage of C144 rises gradually from –15V due to discharging, pin 2 does not reverse since pin 4 of IC23 has reached 0V. The output (Fig. 13-4) of this envelope generator is applied to the base of Q72 and converted exponentially by Q72 together with the signals applied to the base of Q71 (offset ad), signal from TM3 and accent signal via D68, C143 and R362. The converted signal is applied from the collector of Q72 to pin 1 of IC22 to change the amplitude of noise from the filter IC21.

Note: IC23 (AN6912) is constructed with open collector NPN transistors for output and operates on single (negative) power only.

MA White noise is gated by Q65 and supplied to the same buffer IC19 as for the CP sound generator through the filter Q68. Envelope for MA sound generator is generated by Q66 and Q67.

CB
This sound generator uses the outputs of two square waveform oscillators with different frequencies (by Schmitt triggers). Each oscillation output passes the corresponding exclusive gate (VCA, Q14, Q15) and mixed by the filter IC2.

A series of R82 and C34 connected in parallel with CB forms an envelope having abrupt level decay at the initial trailing edge to emphasize attack effect.

CY
The combined square wave outputs of six Schmitt triggers including two for CB generator are separated into high and low range components by two filters composed of IC3. The high range component from pin 7 of IC3 is further separated into two frequency ranges. The output of the gate Q16 has the highest frequency component of this sound generator. Its decay time is short. The output of Q17 is in a frequency range slightly lower than the above output, and its decay time is controllable.

These three signals with different frequency ranges are outputted with their level ratio controlled by VR4.

OH
The high frequency range component signal obtained by the above 1/2 IC3 is gated by Q27 and supplied to the buffer IC7 through the filter Q26. When the CLOSED HI-HAT (CH) is triggered while the OH circuit is activated, Q23 turns on by the voltage applied through R173. At this moment, the decay time of the OH circuit terminates.

CH
This shares the same sound source with the OH. The signal is gated by Q30 and supplied to the filter Q31 and the buffer IC7 (1/2).
TROUBLESHOOTING

This section describes fundamental approach to isolate defective circuits or components.

Although most TR-808 circuits function under the CPU control, possible reasons will often be found on peripheral circuits. Replace CPU last of all. Some useful information can be derived from the circuit description.

DC SUPPLY

Confirmation of DC supply voltages is the first thing to be done in troubleshooting. Check 5V, 25V and back-up, CPU is forced to reset and is not allowed to restart when DC source is so irregular that Voltage Change Detector keeps reset signal.

Lower impedance load connecting to voice output jack can draw relatively large current through op amp when the sound level is high. The sum of the currents, when many louder voices are outputted in step, flowing into these loads would cause DC source to drop enough below the Detector sensing level. To make sure of this, pull all plugs off the jacks. Contrast the above is a short-circuiting IC. One short circuit in a stage only could not be sensed by the detector since "F" supplied to a particular circuit group is independently filtered, or rather, the short circuit will increase ripples in the line, causing TENVU CLOCK to be unstable.

STATUS, SWITCH SCANNING

Each port at PH routes scanning signal to the switches connecting to its bus. PA and PB read signals coming via the switches. If a switch is misread, check switchings for other switches: one sharing the same PH bus, one sharing the same input port — with corresponding switchings.

RAM STORED DATA

As shown in memory map on page 4, a RAM is partitioned into blocks. It is unlikely to occur in a RAM that only one block fails to handle data when the RAM or the Decoder malfunction. For example, if all instrument data but Cow Bell enter IOS, similar phenomenon might true to other RAMs, were the trouble through IO-0 bus.

TRIGGER PULSE

Lack of trigger pulse from a gate is not what Common Trig is responsible for, when other sound generators are fired.

Common Trig with pulse width longer or shorter than 1ms will be a cause of deteriorative voices.
**DESIGN CHANGES & IMPROVEMENTS**

The reasons for modifications will help to remedy the problems as described below, may be found on early TR-808.

Some of the modifications were done at the factory on some products bearing serial number earlier than indicated:

- **MAIN BOARD** - modification 1, 4
- **VOICING BOARD** - modification 1

### MAIN BOARD

<table>
<thead>
<tr>
<th>EFFECTIVE WITH SERIAL NUMBER</th>
<th>PART AFFECTED</th>
<th>REASON (* SOLUTION)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 000300</td>
<td>INT CLOCK 101 (HDI4584) 0.068</td>
<td>Variations in HDI4584 hysteresis sometimes deviate Clock Rate out of specified frequency range. * To down = 0.047+0.039 in parallel * To up = remove 0.039</td>
</tr>
<tr>
<td>2 010600</td>
<td>CF (Hand Clap) 1021 R346 1K R352 22K</td>
<td>CF sound overmatches the rest in level. * Reduce the gain <em>(Both proper and reverberation components.)</em></td>
</tr>
<tr>
<td>3 010600</td>
<td>CPU (pin 30) R01 15K</td>
<td>Small resistance allows CPU to draw relatively larger current from back-up batteries with MODE selected other than PLAY or MANUAL PLAY in Power OFF. * Increase resistance</td>
</tr>
<tr>
<td>4 010600</td>
<td>DIN SOCKET (pin 5) R25 220K</td>
<td>Reject unnecessary signals from external circuitry to prevent false triggering at subsequent stage. * Increase resistance</td>
</tr>
<tr>
<td></td>
<td>CPU (pin 37) Capacitor 0.01uF series DIN pin 2 and chassis Grounding</td>
<td>Protect CPU against static electricity build-up at external circuitry. * By pass charge</td>
</tr>
<tr>
<td>5 010600</td>
<td>NOISE GENERATOR (1024) R129 350K short R511 330K 100K R127 4.7K 10nC0200) C202 0</td>
<td>Variations in UDC4558 bias current are transferred to 1/2 1024 output as an offset reducing gain margin. * Decouple DC</td>
</tr>
</tbody>
</table>

### VOICING BOARD

<table>
<thead>
<tr>
<th>EFFECTIVE WITH SERIAL NUMBER</th>
<th>PART AFFECTED</th>
<th>REASON (* SOLUTION)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 000300</td>
<td>COW BELL (101) C6 0.02</td>
<td>Difficulty in setting COW BELL sound frequency within the specified range. * Extend TIM1 and TIM2 control range</td>
</tr>
<tr>
<td>2 010600</td>
<td>G1-Q4 2SD949F 2SC2021A</td>
<td>To have a clearance between Switch Board and transistors' top.</td>
</tr>
<tr>
<td>3 051850</td>
<td>G5-Q8 2SA733F 2SA337Q</td>
<td>* Employ transistors in shorter package</td>
</tr>
</tbody>
</table>