SSM-2100
MONOLITHIC LOG/ANTILOG AMPLIFIER

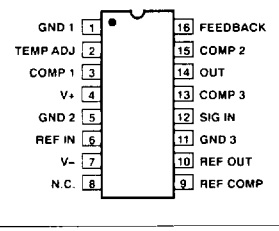
FEATURES
- Performs Log, Antilog, and Log Ratio Functions
- 50pA Input Bias Current (Trimmed)
- 4mV Input Offset Voltage
- On-Board Reference
- Temperature Stabilized
- 25ppm/°C Reference Drift
- 30ppm/°C Scale Factor Drift
- 0.25% Conformance
- 3-Decade Dynamic Range (Voltage Mode)
- 6-Decade Dynamic Range (Current Mode)
- Low Cost

APPLICATIONS
- Photodiode Preamplifier
- Absorption Measurement
- Low Sweep Generators
- High Resolution Data Acquisition
- Analog Computation Circuits
- Analog Compression/Expansion
- Linear-to-dB Conversion

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 16-PIN	
SSM2100P	−10°C to +55°C

PIN CONNECTIONS

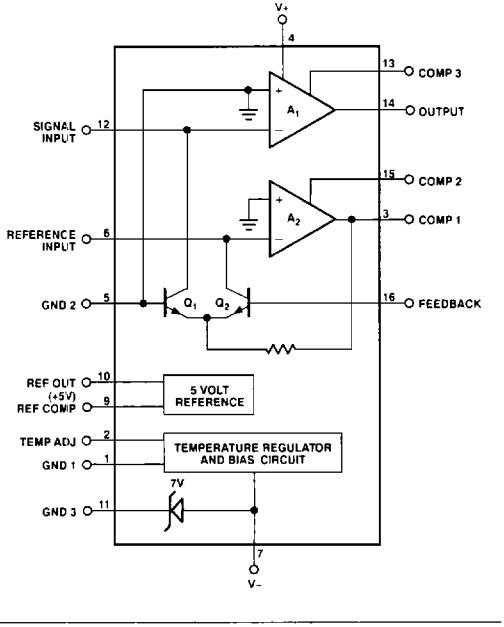


16-PIN PLASTIC DIP
(P-Suffix)

GENERAL DESCRIPTION

The SSM-2100 is a monolithic low-cost DC logarithmic amplifier capable of implementing log/antilog as well as log ratio transfer functions. This device offers a dynamic range of 6 decades of current and 3 decades of voltage. The circuit contains two precision operational amplifiers, a high conformance transistor pair and a precision bandgap voltage reference. An on-board substrate temperature regulator stabilizes both the scale factor and reference drift. A negative voltage reference is also available to facilitate external trimming.

BLOCK DIAGRAM



The SSM-2100 is mask work protected under the Semiconductor Chip Protection Act of 1983.

BSOLUTE MAXIMUM RATINGS

ıpply Voltage ..... 36V or ±18V
nction Temperature ..... +150°C
ɔerating Temperature Range ..... −10°C to +55°C
ɔrage Temperature Range ..... −65°C to +150°C
ıximum Current into Any Pin 10mA
ad Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	82	39	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

.ECTRICAL CHARACTERISTICS at V_S = ±15V, R_{LIMIT} = 1.6kΩ, +5°C ≤ T_A ≤ +50°C, I_{REF} = 1mA, unless otherwise noted.

ıRAMETER	SYMBOL	CONDITIONS	SSM-2100 MIN	TYP	MAX	UNITS
ıformity Error Note 1)	V_{ERROR}	I_{IN} = 100nA to 100µA I_{IN} = 10nA to 1mA (Input Offset Trimmed)	– –	0.25 0.4	– –	%
ale Factor	V_{SCALE}	Measured at Pin 16	65	70	75	mV/Decade
ale Factor 'emperature Drift	TCV_{SCALE}		–	30	–	ppm/°C
ut Offset Voltage Note 2)	V_{IOS}		–	4	8	mV
ut Bias Current Notes 1, 2)	I_B		–	500	2000	pA
lput Offset Voltage	V_{OOS}	$I_{IN} = I_{REF}$ = 1mA Scale Factor Set at 1V/Decade	–	30	70	mV
ver Supply ejection Ratio Note 3)	PSRR	+12V ≤ V+ ≤ +17V −12V ≥ V− ≥ −17V Scale Factor Set at 1V/Decade	– –	500 250	– –	µV/V
put Voltage Swing	V_{OUT}	R_L ≥ 10kΩ R_L ≥ 2kΩ	−1 −0.2	– –	+10 +10	V
erence Output Voltage	$+V_{REF}$	No Load	4.7	5.0	5.2	V
erence Output Voltage emperature Coefficient	TCV_{REF}		–	25	–	ppm/°C
erence Output Current	I_{OUTREF}		5	–	–	mA
erence Load Regulation		R_L ≥ 1kΩ	–	0.015	–	%/mA
erence Supply Rejection	$PSRR_{REF}$	+12V ≤ V+ ≤ +17V	–	0.04	–	%/V
age at Pin 7	$+V_{REF}$		6	7	8	V
ıtive Supply Current	$+I_{SY}$	T_A = +25°C T_A = +50°C T_A = +5°C Heater Disabled	– – – –	35 20 50 5	– – – –	mA
ative Supply Current	$-I_{SY}$		–	5	6.25	mA
ter Start-up Current	I_{HTR}		–	80	120	mA
ulated Chip mperature	T_{REG}		53	60	75	°C

ES:
ıaranteed by design but not directly measured.
plies to both signal and reference inputs.
ferred to output in log mode, or to input in antilog mode.
ecifications apply after a 50 second warmup period.

Specifications subject to change; consult latest data sheet.

7
SSM AUDIO PRODUCTS

GENERAL PRINCIPLE OF OPERATION

The SSM-2100 utilizes the predictable logarithmic relationship between the collector currents and differential input voltage of an NPN transistor pair, given by:

$$\text{delta } V_{IN} = kT/q \ \ln \ I_{C2}/I_{C1} \quad (1)$$

where: k = Boltzmann's constant (1.38×10^{-23}) J/°K)

q = charge of an electron (1.6×10^{-23} C)

T = absolute temperature (°K)

Deviation in the absolute temperature term is eliminated with the SSM-2100 design since the chip temperature is regulated at +60°C (333°K).

PRINCIPLE OF LOG OPERATION

The logging function is realized by placing the antilog element (transistor pair) in the feedback loop of the output converter amplifier (A_1) as shown in the block diagram. As shown in Figure 1, the loop is closed and the conversion is scaled with feedback resistors R_1 and R_2 from pin 16 to pin 14. The high-gain op amps (A_1 and A_2) have negligible input bias current. These force the collector currents of the high conformance transistor pair to be equal to the input current (pin 12) and the reference current (pin 6).

Referring to equation (1), the input current becomes I_{C1} and the reference current I_{C2}, while delta V_{IN} is V_{BASE} Q_2 or V_{16}, since the base of Q_1 is ground. Here, the output amplifier A_1 forces the base of Q_2 to be at the appropriate voltage governed by equation (1) and the collector currents of Q_1 and Q_2. With the reference current set at 1mA, the input current operates at less than or equal to 1mA. In the case of the inverting log amp, as the input current decreases, the V_{BE} of Q_1 decreases which increases V_{16} or V_{OUT} since the V_{BE} of Q_2 is fixed.

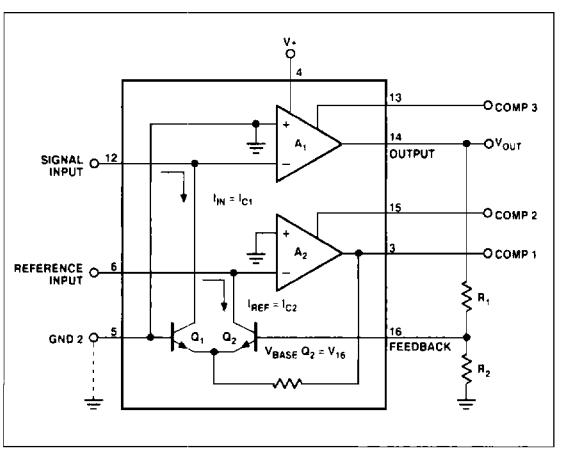


FIGURE 1: *Basic Principle of Operation*

NOTE: The output amplifier can only swing to approximately 1.5V below ground and sinks about 300µA. For this reason, they are used only with positive output voltages. For bipolar amplifier output, see Figure 7 in the Log Ratio section.

Equation (1) can be rewritten:

$$V_{16} = kT/q \ \ln \ (I_{REF}/I_{IN}) \quad (2)$$

converting to base 10:

$$V_{16} = 2.303 \ kT/q \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (3)$$

Figure 1 shows the feedback which produces the output scale factor:

$$V_{OUT} = V_{16} \ (R_2/(R_1 + R_2)) \quad (4)$$

Substituting into equation 3 yields:

$$V_{OUT} = 2.303 \ kT/q \ (R_1 + R_2)/R_1 \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (5)$$

Letting $\mathbf{K} = 2.303 \ kT/q \ (R_1 + R_2)/R_2$ (6)

or $\mathbf{K} = 0.066 \ (R_1 + R_2)/R_2$ (usually set to 1V/decade with R_2 = 470Ω)

For current-mode operation:

$$V_{OUT} = \mathbf{K} \ LOG_{10} \ (I_{REF}/I_{IN}) \quad (7$$

For voltage-mode operation:

$$V_{OUT} = \mathbf{K} \ LOG_{10} \ (V_{REF}/V_{IN} \times R_{IN}/R_{REF}) \quad (8$$

Since both op amp inputs rest at virtual ground, the reference and input currents can easily be generated by applied voltages through external resistors without generating excessive errors

For the best results, the input and reference currents should be kept below 1mA.

A 5V reference has been included on chip for applications requiring a true log function (rather than a log ratio function).

INPUTS

As with all log amplifiers, the SSM-2100 has a limited dynamic range of 3 decades for voltage inputs. This is partially due to input offset voltage (trimmable) and various second order effects.

For the widest dynamic range, current-mode operation is recommended. The device can handle 5 decades of current input untrimmed and at least 6 decades when trimmed. Similarly, when operating in the log ratio mode, the device can handle 1 decades and 12 decades, respectively.

In order to ensure unconditional stability when operating with true current inputs, it is important to shunt the signal input to ground with a 10kΩ resistor and a 10nF capacitor.

NEGATIVE POWER SUPPLY CONSIDERATIONS

Because the negative power suppply is regulated at –7V, it is necessary to add a current limiting resistor (R_{LIMIT}) in series with pin 7. When using –15V for V–, a value of 1.6kΩ is recommended for R_{LIMIT}. This will keep the voltage at pin 7 very stable and useful for external trimming. Note that the negative power supply is internally regulated and needs no decoupling.

POSITIVE POWER SUPPLY CONSIDERATIONS

Because of the high gain of the temperature regulator circuit, generous positive supply decoupling should be used. The 0.2μF decoupling capacitor shown on the application circuits should be of ceramic type and mounted as close to pins 1 and 4 as possible. It should also be noted than pin 1 carries all the heater current and care should be taken when laying out ground lines to prevent this from causing errors.

TEMPERATURE CONTROL

The internal chip temperature is regulated at about 60°C if the temperature adjustment (pin 12) is not used. This on-board substrate temperature regulator stabilizes the scale factor and reduces drift of the reference.

The regulated chip temperature can be increased or decreased by the use of pin 2. To decrease the temperature by n°C, connect a resistor of the value 3.5n MΩ between pin 2 and 10. To increase the temperature by n°C, connect a resistor of the value 3/n MΩ between pins 2 and 7.

In some applications such as those requiring low power, the temperature regulator can be disabled entirely. This is accomplished by connecting a 100kΩ resistor between pins 2 and 4 (V+). In this case, the reference drift is about 70ppm/°C. The scale factor drift can be compensated by using a temperature compensating resistor* instead of R_2.

APPLICATIONS

The SSM-2100 can be connected for voltage or current logging functions. Figures 2a and 2b show the transfer characteristics of the inverting log amplifier for current and voltage mode operation.

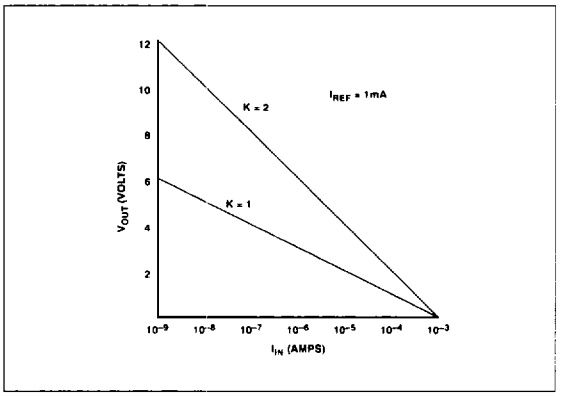


FIGURE 2a: *Inverting Log Amp with Current Input*

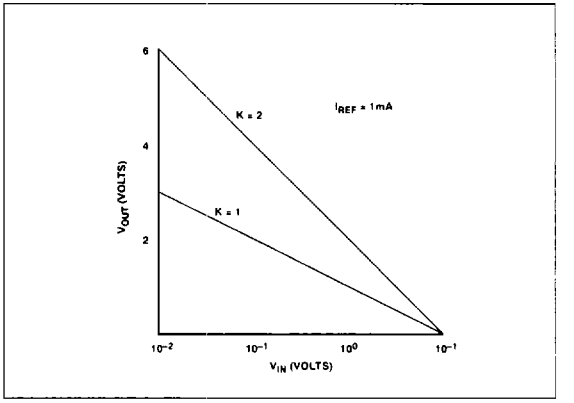


FIGURE 2b: *Inverting Log Amp with Voltage Input*

INVERTING LOG AMPLIFIER

Figure 3 shows the SSM-2100 configured in the inverting log mode. Setting $I_{IN} = I_{REF}$ with $V_{IN} = 10V$, the output will be zero and increase by 1V/decade as I_{IN} is decreased. Whereas V_{IN} can be varied proportionally by varying R_{IN}, a 10V input optimizes the dynamic range with ±15V supplies.

To vary the scale factor, it is best to change R_1. To alter the output offset at a given input voltage, adjust R_{REF}. Phase compensation for the circuit is provided by C_1, C_2 and C_3. This scheme yields 30kHz small-signal bandwidth at 1mA input current, 8kHz at 1µA and approximately 1.6kHz at 100nA.

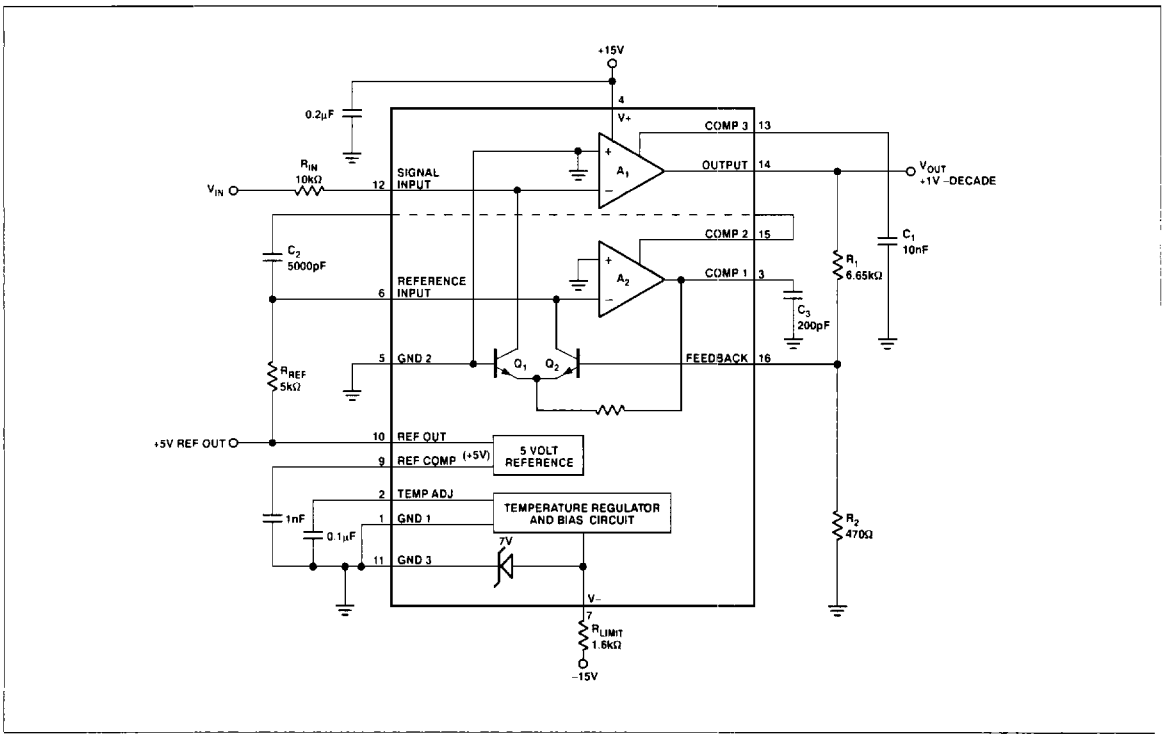


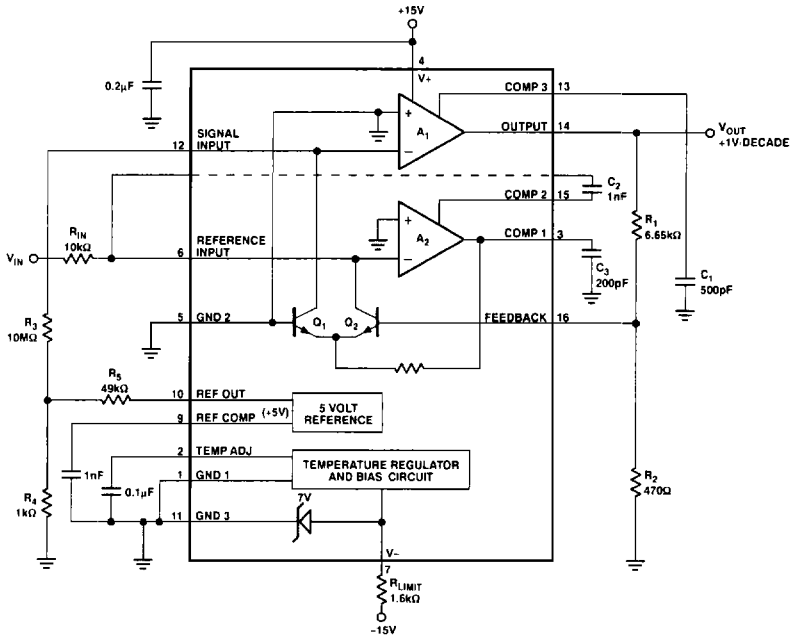
FIGURE 3: *Inverting Logarithmic Amplifier*

NONINVERTING LOG AMPLIFIER

Interchanging the signal and reference inputs yields a noninverting log amplifier as shown in Figure 4. In this configuration, the output crosses zero when the input is five decades below the full-scale value. This can be adjusted by varying R_3.

R_1 and R_2 can cause a slight inaccuracy because they add to the base resistance of Q_1 and Q_2. This can be minimized by keeping R_1 and R_2 as small as possible. It is recommended that $R_2 = 470\Omega$.

The small-signal bandwidth of this circuit is 5kHz with inputs currents from 1μA to 1mA. Over the full 5-decade input current range, the bandwidth is better than 2kHz.



IGURE 4: *Noninverting Logarithmic Amplifier*

ANTILOG AMPLIFIER

Figure 5 shows the configuration for the antilog amplifier. The input range for this circuit is zero to 10V which can be adjusted by R_1. The output scale factor is 1V/decade which can varied by adjusting R_{OUT}.

The transfer function is also derived from equation (1). In the antilog configuration, the current I_{C1} becomes I_{OUT} and V_{BASE} Q_2 or V_{16} is $V_{IN}(R_2/(R_1 + R_2))$. Equation (2) now becomes:

$$V_{IN}(R_2/(R_1 + R_2)) = kT/q \ \ln(I_{REF}/I_{OUT}) \quad (9)$$

or

$$I_{REF}/I_{OUT} = \exp[R_2/(R_1 + R_2) \ q/kT \ V_{IN}]$$

or

$$I_{REF} R_{OUT} = V_{OUT} \exp[R_2/(R_1 + R_2) \ q/kT \ V_{IN}]$$

converting to base 10 and letting K = 2.303 kT/q $(R_1 + R_2)/R_2$ or $0.066(R_1 + R_2)/R_2$ (assuming T = +60°C or 333°K)

the final antilog transfer function becomes:

$$V_{OUT} = I_{REF} R_{OUT}/10^{[VIN\ R2/.066\ (R1\ +\ R2)]}$$

or

$$V_{OUT} = I_{REF} R_{OUT}/10^{[VIN/K]}$$

To set K = 1V/decade, $R_2/(R_1 + R_2) = 0.066$

If $R_2 = 470\Omega$, $R_1 = 6.65k\Omega$

The bandwidth of the antilog amplifier circuit is approximately 500kHz.

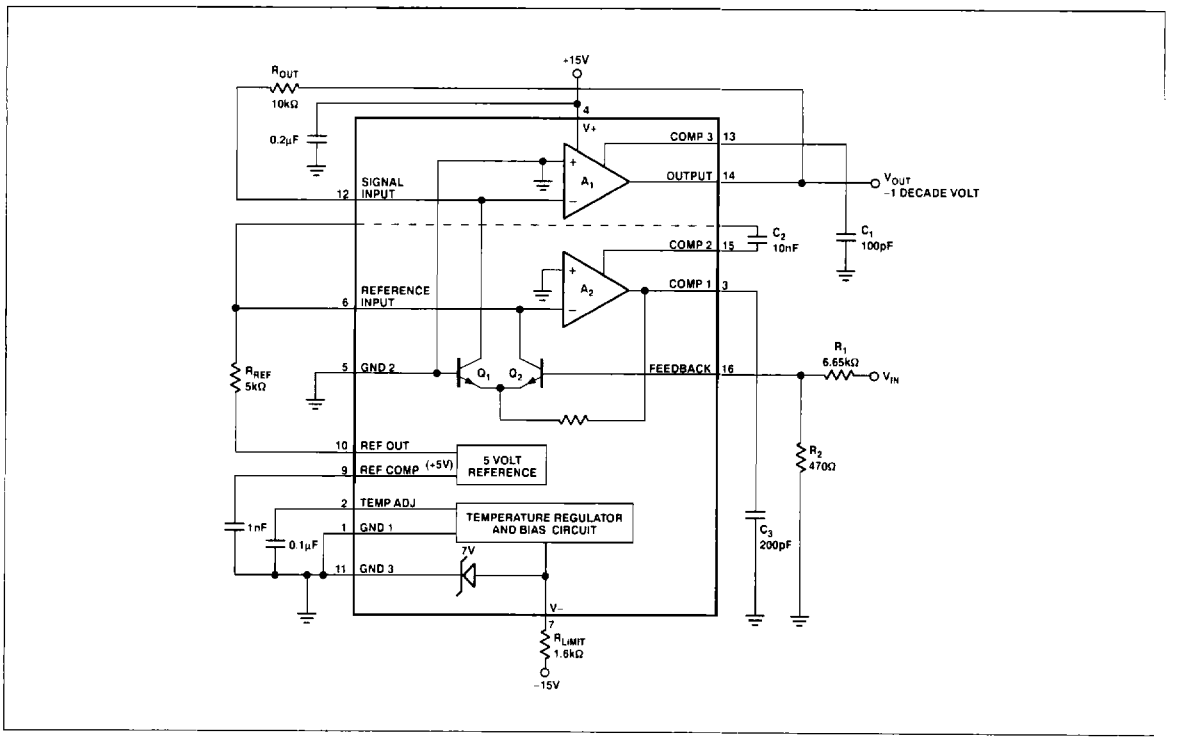


FIGURE 5: *Antilogarithmic Amplifier*

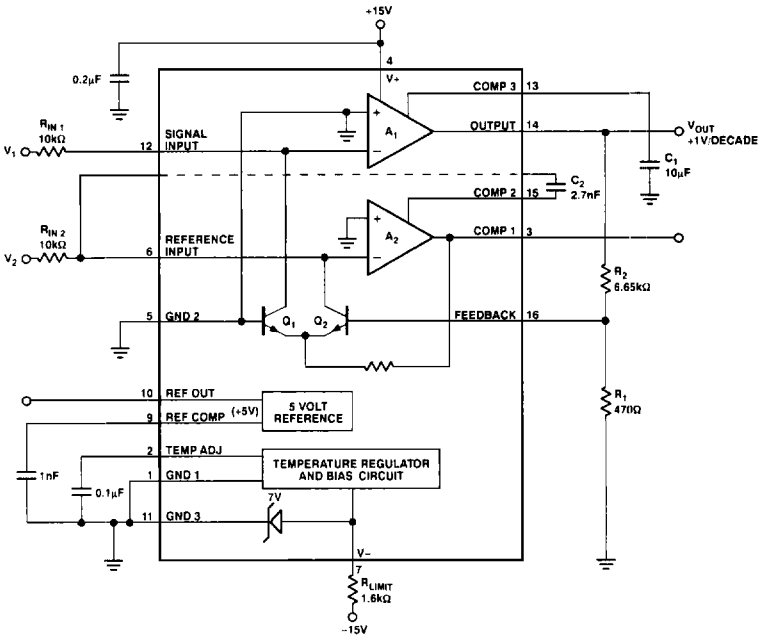


FIGURE 6: Log Ratio Amplifier, $V_{OUT} = K \log (V_2/V_1)$, K = 1V/Decade with Values Shown

OG RATIO AMPLIFIER

he output of the log ratio amplifier is proportional to the ratio of s two input signals. The SSM-2100 is very well suited to this pplication because both the signal and reference inputs oper- te at true virtual ground. This eliminates the need for an exter- al true current source as required by other types of log amplifi- 's.

he log ratio amplifier shown in Figure 6 has a dynamic range of $)^5$ to 10^{-1} if the output buffer of Figure 7 is not used. This is ecause the output amplifier (A_1) can swing to a minimum of)out 1.5V below ground and can only sink about 300µA maxi- um. Thus, the input current should not be more than one dec- de below the reference current.

)r full four-quadrant operation, however, refer to the output uffer of Figure 7. The addition of this circuit will provide a ±5V utput for reference/signal ratios from 10^5 to 10^{-5} for a full 10- ecade range.

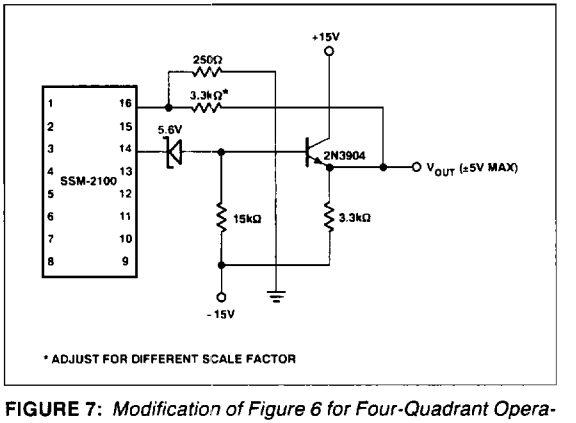


FIGURE 7: *Modification of Figure 6 for Four-Quadrant Operation*

TRIMMING THE SSM-2100

Figure 8 shows the general trimming technique for the log and log ratio applications shown in Figures 3, 4 and 6. The trim schemes for scale factor (R_1), input offset (R_x, R_y), and output offset (R_{REF}) factor are shown. For log ratio applications, the input offset trim can be duplicated for the reference input.

The scale factor trim scheme is identical in all applications. Simply replace R_1 with a 6.2kΩ resistor and 1kΩ potentiometer.

Input offset trimming removes errors from input bias current as well as amplifier offset. For optimum trim integrity, the use of the positive and negative reference voltages yields high rejection to variations in power supply voltages.

Output offset errors are essentially due to the mismatch between the base-emitter voltages of Q_1 and Q_2. The output offset adjustment (R_{REF}) scheme shown applies to the inverting log amp and the antilog amplifier. Output offset is adjusted in the noninverting log amplifier by changing R_5 in Figure 4. To adjust out the equivalent error in the log ratio amplifier, replace either of the 10kΩ input resistors with a 9kΩ resistor and 2kΩ potentiometer.

Unlike an operational amplifier, a log amp can not be trimmed with V_{IN} = 0 since the log of zero would theoretically produce an infinite output voltage.

LOG AMPLIFIER TRIM PROCEDURE

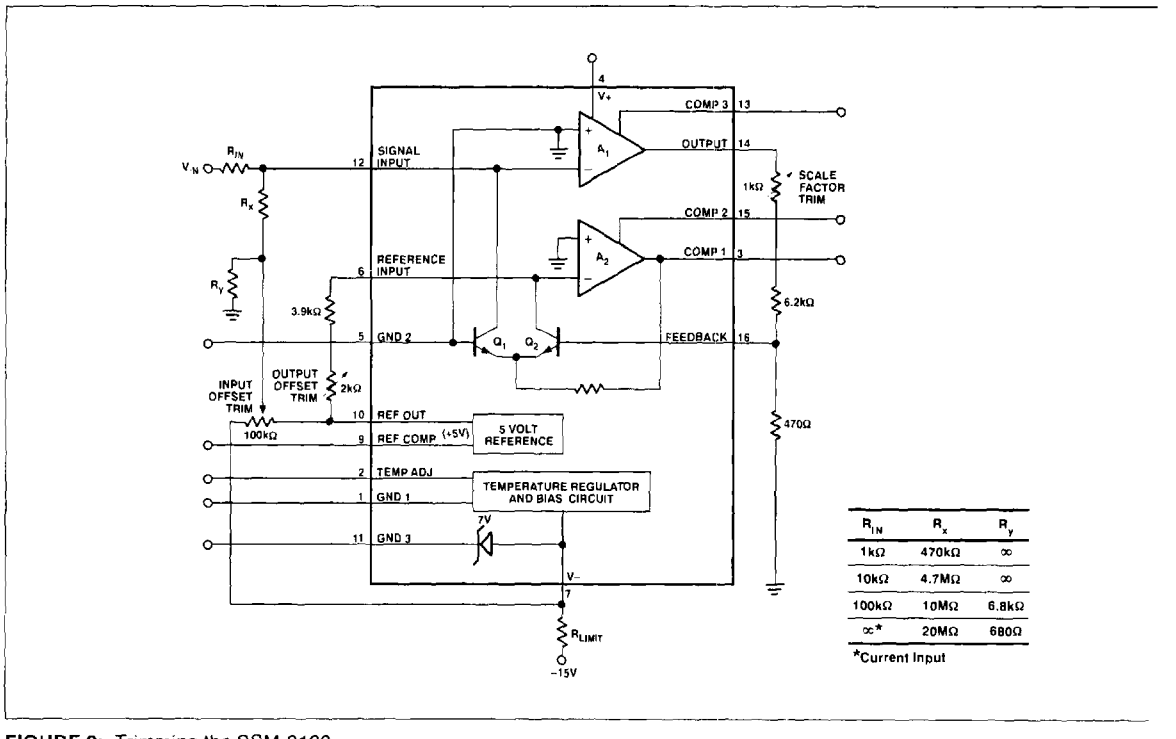
Log amp trim for K = 1:

1. Apply full-scale input voltage or current and adjust output offset for the proper output.
2. Apply an input signal one decade down from full-scale and adjust the scale factor for the desired output.
3. Finally, with the minimum input signal applied, adjust the input offset trim for the correct minimum scale output voltage or current.

ANTILOG AMPLIFIER TRIM PROCEDURE

Antilog trimming for K = 1:

1. Set full-scale by grounding V_{IN} and adjusting the output offset trim until V_{OUT} is 10V.
2. Apply 1V to V_{IN} and adjust the scale factor for 1V output.
3. Set the V_{IN} to the maximum value to be used and adjust input offset trim for the minimum desired output. Using K = 1, adjust for V_{OUT} of 0.1V with V_{IN} at 2V.



R_{IN}	R_x	R_y
1kΩ	470kΩ	∞
10kΩ	4.7MΩ	∞
100kΩ	10MΩ	6.8kΩ
∞*	20MΩ	680Ω

*Current Input

FIGURE 8: *Trimming the SSM-2100*